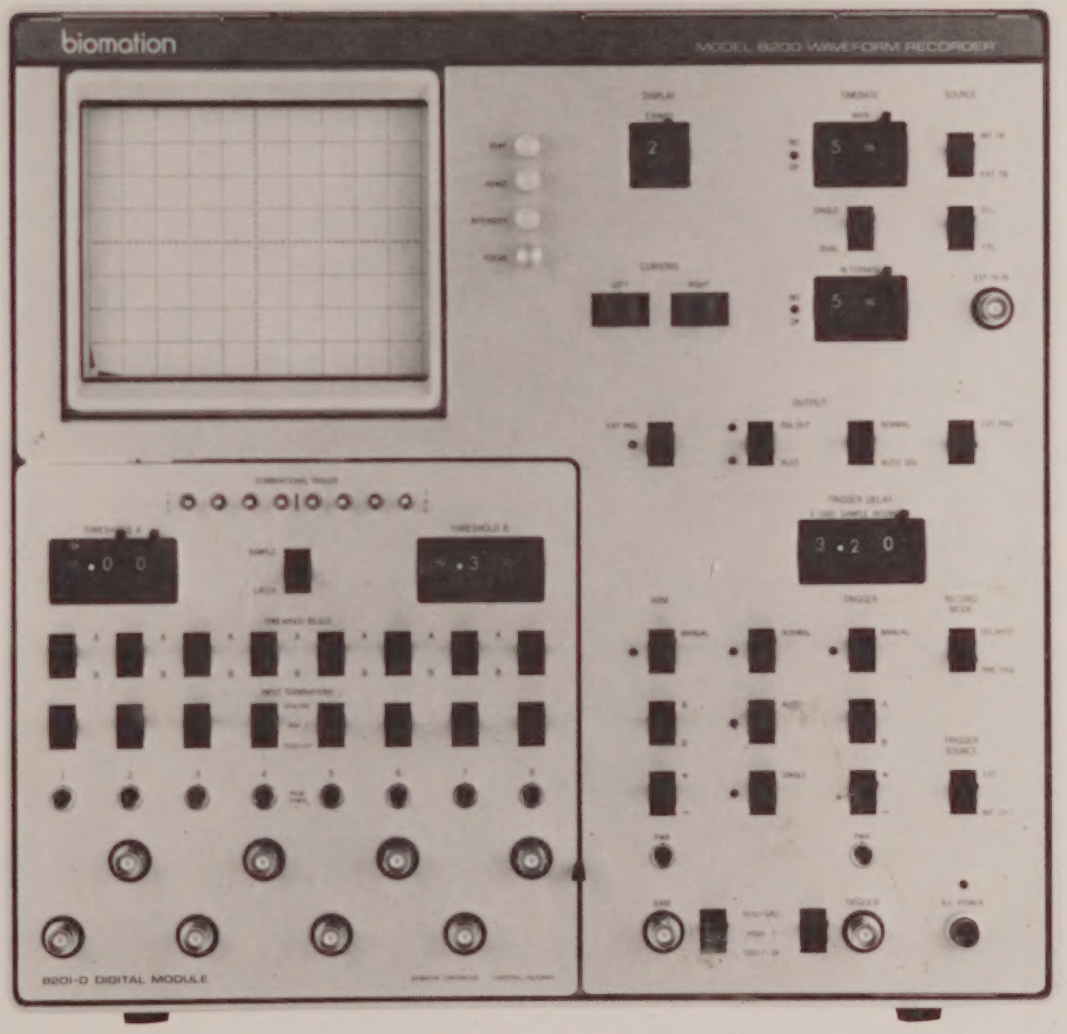
Part No. 0850-0300

MODEL 8200
DIGITAL LOGIC RECORDER



OPERATING AND SERVICE MANUAL

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MODEL 8200
DIGITAL LOGIC RECORDER

OPERATING AND SERVICE MANUAL

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SUPPLEMENT A

8200 DIGITAL MODULE PLUG-IN

The information in this supplement pertains only to those units with the 8200 Digital Module plug-in. To aid the user in filing this material, the pages were numbered to show where they should appear in the manual. The sections affected are IV, VII, and IX.

4.23 8200 Digital Module plug-in functions; refer to Figure 4.1

(1) Input Connectors

Eight connectors for input of as many digital signals. Input impedance 50 Ω to ground. Maximum input ±4 V.

(2) PWR Connectors

Provides ±15 V and ground for powering active FET probes. For connector pin designations, refer to Digital Module plug-in schematic in Section IX.

(3) A/B

Allows selection of Threshold A or B reference for each channel.

(4), (5) THRESHOLD A, B

Permits selection of two different threshold levels so that two different logic families may be observed during one record sweep, or two thresholds may be selected for one family. Range of adjustment is ±2.975 V, in increments of 25 mV. Maximum amplitude hysteresis is 25 mV.

(6) SAMPLE/LATCH

In SAMPLE position, the unit compares input levels with the preselected threshold level and stores a high or low, as appropriate, on the active clock edge, simultaneously on all channels. Maximum skew between channels is 1 nsec. Minimum pulse width always detected and recorded is one clock interval plus 1 nsec, with 200 mV, or greater, overdrive. Thus, the data stored in memory reflects the input states at the clock transition.

In the LATCH mode, the unit stores as above for single threshold transitions in a clock period. In addition, pulses shorter than one clock interval that occur between active clock edges cause the input threshold detector to latch in a complementary state from that at the previous active clock edge. This changed state is stored in the memory at the next active clock edge. This latch acts as a detector of fast pulses and presents them in the time cells immediately following their actual occurrence. This input latch function may cause the latched data to be stored in one or two time cells following the detected pulse. Short pulses or data transitions occurring during adjacent clock time intervals may be merged in the recorded data. Minimum pulse width always detected in Latch mode is 3 nsec with 200 mV or more threshold voltage overdrive. Typical minimum is 2 nsec.

OPERATING & SERVICE MANUAL

MODEL 8200

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SECTION I

GENERAL INFORMATION

1.1 Certification

Biomation Corporation certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. No other warranty is expressed or implied. We are not liable for consequential damages. For full warranty statement, see back of manual.

1.3 Instrument Description

The Model 8200 Waveform Recorder is a compact solid state electronic instrument that can be configured to operate as a Digital Logic Recorder, or as a Transient Recorder, depending on the plug-in unit selected by the user. The discriminated digital or converted analog data is stored digitally in memory.

The mainframe functions in the same manner regardless of the plug-in with which it is equipped. The integral CRT display not only permits viewing of the memory contents with horizontal expansion factors up to X100, but also provides two cursors and alphanumeric readout. An analog output is available for an external CRT, or a flatbed plotter.

Also, the unit may be interfaced, with suitable coupling circuitry, to a variety of digital computers, time share terminals, magnetic tape storage devices, etc., as a part of a data acquisition system.

The Model 8200 is a bench-type instrument with tilt-up stand. Specifications are shown on the following pages.

1.4 Specifications

The following performance characteristics and specifications are for the Model 8200 Waveform Recorder mainframe in unit with the 8201-D Digital Module plug-in:

SIGNAL INPUTS

Channels. 8

Impedance. Selectable for each input: 50 Ω to −2V, 50 Ω to ground, 1MΩ//30pf to ground. Probe power connectors provided for use with FET active probes.

Threshold Levels. Selectable A or B for each channel. A and B levels individually adjustable from −2.975 to +2.975 V in increments of 25 mV. Maximum amplitude hysteresis is 25 mV.

Maximum Input Voltage. 50 ohm inputs: ±4V
1 mohm inputs: ±50V

Input Modes. Selectable: SAMPLE or LATCH

SAMPLE. Unit stores the detected input logic level at the active clock edge for each clock cycle simultaneously on all input channels. Maximum Channel-to-Channel time skew of this clocked data is 1 nsec. Minimum pulse width always detected and recorded is one clock interval plus 1 nsec. with 200 mv or more threshold voltage overdrive.

LATCH. Pulses shorter than one clock interval which occur between active clock edges cause the input threshold detector to latch in a complimentary state from that at the previous active clock edge. This changed state is stored in the memory at the next active clock edge. This latch acts as a detector of fast pulses and presents them in the time cells immediately following their actual occurrence. This input latch function may cause the latched data to be stored in one or two time cells following the detected pulse. Short pulses or data transitions occurring during adjacent clock time intervals may be merged in the recorded data. Minimum pulse width always detected in Latch mode is 3 nsec. with 200 mv or more threshold voltage overdrive. Typical minimum is 2 nsec., see figure 1.

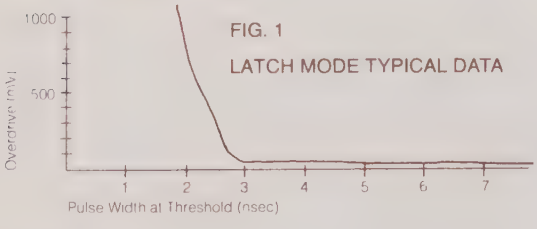


FIG. 1

LATCH MODE TYPICAL DATA

TIMEBASE AND MEMORY

Sample Interval. Selectable: INTERNAL or EXTERNAL source.

INTERNAL TIME BASE. Single or dual rates independently selectable from 5 seconds to 5 nsec in a 1-2-5 sequence.

EXTERNAL TIME BASE. Selectable TTL or ECL logic level and termination for rates to 200MHz. Fixed delay between input data signals and external clock input at the input threshold detectors is typically 12 nsec. with the ECL clock input selected and 17 nsec. with the TTL clock input selected.

Memory Size. 2048 words with 8 bits per word.

ARM FUNCTION

Source. Selectable: MANUAL (with LED "ready" indicator) or EXTERNAL.

Level. Selectable: A or B signal threshold levels.

Slope. Selectable + or −

External Input. Front panel BNC with adjacent FET probe power connector. Selectable input impedance: 50 Ω to −2V, 50 Ω to ground, 1MΩ//30 pf to ground.

TRIGGER FUNCTION

Source. Selectable: MANUAL (with LED ready indicator), INTERNAL from combinational switches (any channel or parallel word), or EXTERNAL.

Level. Selectable, A or B signal threshold levels.

Slope. Selectable + or −

Settable Delay. Selectable in increments of 10 record clock intervals to 9990 record clock intervals.

Static Delay. With Delayed Record Mode selected and the Settable Trigger Delay at zero, the fixed delay between the detected trigger and the first data stored in the memory is typically 8 record clock intervals plus 70 nsec.

Jitter. Data from repetitive record cycles with respect to the input signals will exhibit the following maximum time jitter:
Delayed Record Mode: 3 clock intervals
Pretrigger Record Mode: 9 clock intervals

External Input. Front panel BNC with adjacent FET probe power connector. Selectable input impedance: 50 Ω to −2V, 50 Ω to ground, 1MΩ//30pf to ground.

Trigger Modes. Selectable: AUTO, NORMAL or SINGLE.

AUTO TRIGGER. Automatically provides alternating record and display cycles when Delayed record mode is selected (primarily useful for setup and calibration).

NORMAL TRIGGER. Unit automatically "Armed" to accept each trigger event.

SINGLE TRIGGER. Arm function must be provided prior to each trigger function.

DATA RECORDING

Record Modes. Selectable: DELAYED or PRETRIGGER.

DELAYED RECORDING. Recording begins at delayed trigger event and stops after 2048 words have been stored in memory.

PRETRIGGER RECORDING. Recording begins at the Arm event and stops at the delayed trigger event. Setting of the trigger delay determines the portion of recorded signal which preceeded the trigger.

Dual Timebase Recording. Usable in either Delayed or Pretrigger operation with Internal Timebase selection. Recording begins at Main timebase rate and switches to Alternate timebase as a function of the trigger.

DISPLAY

Vertical Control. Single adjustment for entire field.

Spot Definition. Intensity and Focus controls provided.

Horizontal Control. Single adjustment for entire field.

Cursors. Two Vertical cursors are displayed on each channel's display. Each cursor movable horizontally with individual control to a resolution of one point.

Expansion. Selectable horizontal expansion factors of ×1, ×2, ×5, ×10, ×20, ×50 and ×100. Expansion of ×2 and above is linear beginning with the position of the left cursor. Marking of each clock period for expansions of ×10 and greater.

Display Numerics. CRT display presents numerical readout of the following information: Main sample interval, Alternate sample interval (if Dual timebase selected). Expansion factor and number of clock periods between cursors.

DIGITAL INTERFACE

Programmability. All front panel controls are programmable except display adjustments, input impedance selection switches, combinational trigger switches, power switch and EXT PROG selector switches. Operation of EXT PROG switches places unit under program control.

Program Input. 16 bit parallel TTL levels. Selectable positive or negative true. One-in-eight address assignment and 3-bit address field.

Data Readout. All active front panel control functions except display adjustment, input impedance selection switches, combinational trigger switches, and power switch can be read via the Digital Interface when the unit is not under program control. When under program control, the programmed functions may be similarly read out. In addition, the operational status of the instrument and the data stored in the unit's memory can be read out through the Digital Interface.

Data Output. 8-bit parallel, TTL levels "open" when not "addressed". Selectable positive or negative true. Asynchronous transfer under Flag/Command "handshake" control at rates to 3×10^6 words/second.

Digital I/O Control Signals. Command input, Flag output, TTL levels, selectable positive or negative true.

MISCELLANEOUS

Size. HEIGHT. 15-1/2" (39 cm)
WIDTH. 15-3/4" (40 cm)
DEPTH. 22-3/4" (58 cm)

Weight. Approximately 88 lbs (40 Kg)

Power. 115/230 V rms ±10%, 50-60 Hz
Approximately 250 W

Price: $18450 f.o.b. Cupertino, California

SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage and installation of the Model 8200.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Biomation representative or the Biomation factory.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice. A factory approved shipping carton can also be obtained by contacting Biomation.

2.4 Power Connection

The procedure for selecting the proper operating line voltage is covered in Section 9.5, pages 162 and 163, and also in the accompanying Tektronix Model 604 Operating Manual. These instructions MUST be followed to prevent damage to the unit.

For 115-V operation, use an AGC 4-A fuse. For 230-V operation, use an AGC 2-A unit.

CAUTION: Before plugging instrument in AC power line, be sure line voltage switch is properly positioned.

Power cable: The Model 8200 is equipped with a detachable 3-wire power cable. Proceed as follows for installation:

a) Connect line-cord plug (3-socket connector) to AC line jack at rear of instrument.

b) Connect plug (2-blade with round grounding pin) to 3-wire (grounded) power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety. When only 2-blade outlet is available, use connector adapter, then connect short wire from side of adapter to ground.

2.5 Preparation for Use

The Model 8200 is an integrated, self-contained unit. Data may be captured and visually analyzed using the built-in CRT and cursors. The following sections cover setup, operation, and interface requirements.

2.6 Initial Warm-up

Although the Model 8200 is a solid state instrument, a brief warm-up period of approximately 10 minutes is required for the internal circuitry to reach thermal stabilization.

SECTION III

PRINCIPLE OF OPERATION

3.1 Introduction

The discussion of the operation of the Model 8200 will be limited at this time to the use of the unit with the Model 8201-D Digital Module plug-in. In this configuration, the unit will be known as the Model 8200 Digital Logic Recorder.

The Model 8200 provides the capability required for precise analysis of high speed and complex digital devices. The unit produces a familiar timing diagram presentation of up to eight signals present in a device or system with a time resolution of as short as 5 nsec. The 8200 detects the "one" or "zero" states on all inputs and stores 2048 of these parallel decisions per channel at a selected record rate. The fast, triggered capture, long memory and familiar display features are particularly useful for analyzing the complex I/O functions of current high-speed digital devices and equipment.

A block diagram of the Model 8200 is presented in Figure 3.1.

3.2 Basic Functional Description

The Model 8200 looks and operates much like a multiple input oscilloscope. The trigger selection and detection circuitry and the CRT display and controls are particularly familiar to the 'scope user. In operation, the 8200 detects the state of up to eight digital signals against either of two preset threshold levels, updates the detectors on each cycle of an internal or external clock and sequentially stores 2048 such simultaneous decisions in eight channels of digital memory.

This information is then repetitively read from the memory, converted to "one-bit analog" signals and displayed as a flicker-free timing diagram presentation on the CRT.

Not only does the user have the ability to look at eight signals, but also the signals do not have to be repetitive; i.e., one repetition of a logic sequence of events may be stored and analyzed.

3.21 Input Threshold

The definition of a stored data signal as a binary "1" or "0" is determined by one of two switch selected logic threshold levels. A selection of threshold voltages between $\pm$2.975 V, in increments of 25 mV, is provided.

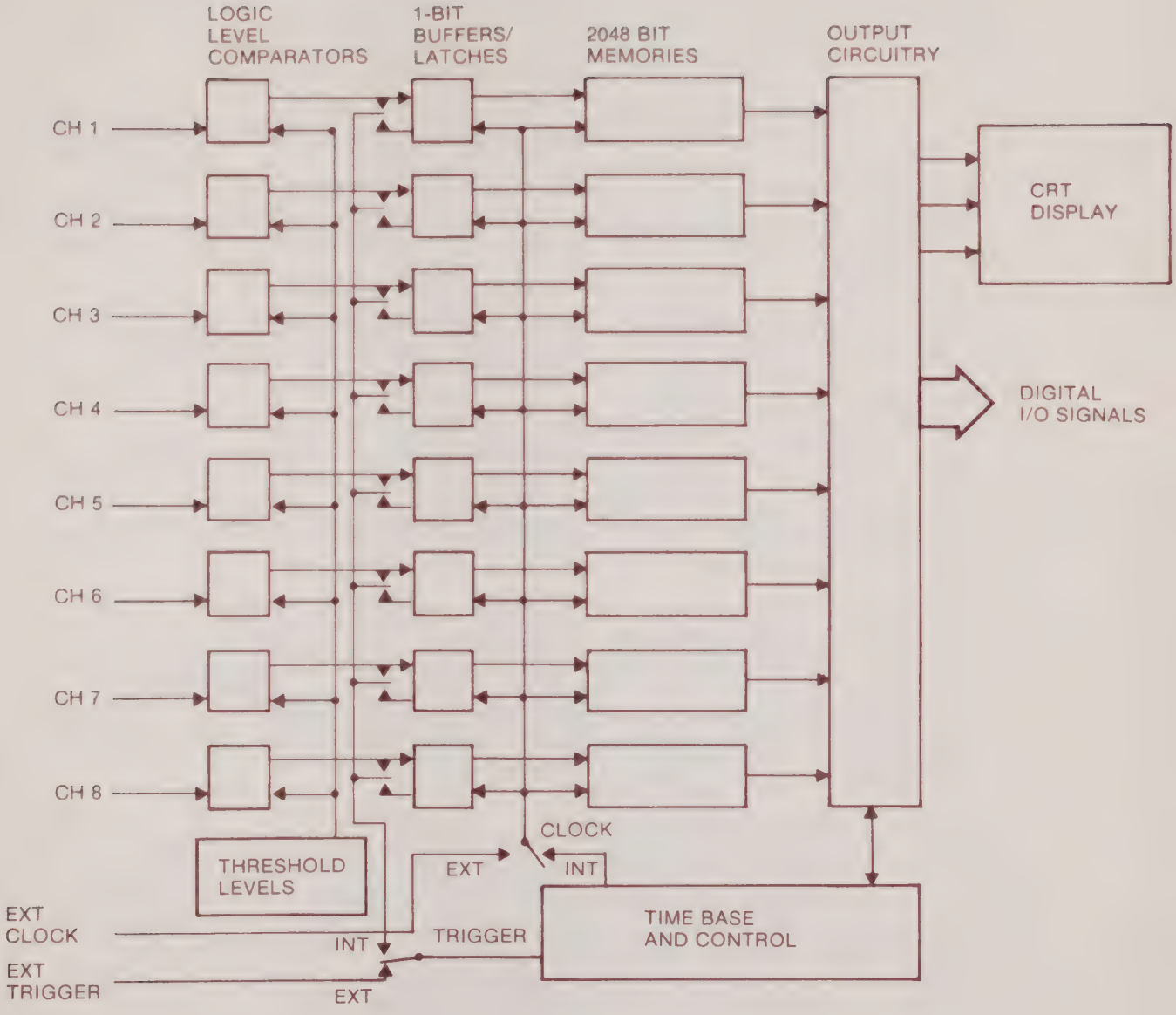


FIGURE 3.1. Model 8200 Digital Logic Recorder Block Diagram

3.22 Sample Mode

In the "SAMPLE" mode of operation, the input levels are strobed into the memory as "1" or "0" based on the signal level with respect to the selected threshold at the time of the rising edge of the clock.

3.23 Latch Mode

The "LATCH" mode of recording permits narrow spikes to be recorded. Any spike (positive or negative) with sufficient amplitude and duration causes an input latch to set. This changes the state of the next bit to be written in memory. In this way, narrow spikes or "glitches" occurring at random times between sample clock transitions can be captured.

Typically, a glitch that exceeds the threshold by 300 mV can be as short as 3 nsec and still be detected.

3.24 Signal Inputs

The eight signal inputs and the Arm and Trigger inputs are all terminated in 50 Ω to ground. A convenient power connector is provided adjacent to each input to power an active FET Probe. See Section IX for the power connector pin assignments.

3.25 Record Rates

The internal sample interval is switch selectable from 5 sec to 5 nsec, in a 1-2-5 sequence. The clock of the device or system under test may be input via the front panel to effect synchronous recording, a distinct advantage when synchronous logic is being examined.

3.26 Normal Record Mode

A Normal record sequence is started by the Trigger function and stops after the entire memory has been refreshed. The trigger function can be derived from one of the input signals or from an external source. The trigger can also be delayed by as much as 9,990 sample intervals in increments of ten sample intervals.

3.27 Pretrigger Record Mode

The Pretrigger record mode is unique and very useful. With the Pretrigger mode selected, the unit begins recording upon receipt of the Arm command and continuously updates the memory with new data (destroying the "oldest" data) much like recording with a tape loop. Recording is stopped by the delayed Trigger. The amount of trigger delay selected

determines the amount of prior-trigger data stored when recording ceases; e.g., selection of a 1000 sample interval trigger delay will cause the unit to continue recording for 1000 samples after the trigger, and then cease recording while retaining 1048 words of contiguous prior trigger data. In this way, eight points in a digital circuit can be continuously monitored, waiting for a specific fault or logic event to trigger the unit. When the trigger occurs and the delay is counted out, a contiguous record of events (before and after the trigger) is recorded and displayed.

3.3 Recording Considerations

As the Model 8200 can record as a function of either the internal clock or an external clock, note must be taken of some basic differences in these two methods.

When the internal clock is used for recording, no particular phase relationship will exist between this clock and any synchronous information rate in the signals being recorded. Therefore, a beat frequency can exist between these two basic rates. If the 8200 internal clock is 10 times or more higher in frequency than the signal rate, very little effect will be noted in the recorded data. For high signal rates (with respect to the record clock), a beat rate effect can be seen by varying widths in the recorded "pulses" and even periodic "dropped" bits when these rates approach the limiting ratio of two to one.

When the synchronous clock used for the generation of the input signals to the 8200 is used as the record clock in the 8200, no phase errors exist and no beat frequencies will be evident; i.e., the beat note is zero frequency. In this case, signals with information rates up to and including 1/2 the clock frequency can be recorded, without distortion. This is called synchronous recording.

Bear in mind that the 8200 is an instrument for the detection and storage of digital data. As such, the unit only discriminates between two different levels as defined by the threshold switches. The data stored and displayed is not an analog representation of the input signals, but a pattern of "ones" and "zeros" that represent threshold crossings.

3.4 Outputs and Control Inputs

3.41 Display Output

Once Record is terminated, the unit automatically goes into a display mode, where the memory is continuously circulated and the contents are repetitively output to the integral CRT.

The display presentation is an eight-trace timing diagram format. With no horizontal expansion, 2048 bits of information per line are displayed, approximately 200 per division.

Two cursors and a horizontal expansion switch (to X100) provide the ability to make a very precise visual examination of the data in memory.

3.42 Plot Output

A slow output of the timing diagram display is available at the rear panel. This enables the user to obtain a hard copy of the memory contents on an X-Y plotter. An X ramp and a Pen signal are also available.

The Y signal is nominally 1 V p-p for the full field of eight traces. Each line of data is plotted sequentially. The numerics at the top of the CRT are not plotted. Various plot rates are strap selectable. See Section VI for details.

The X signal is a ramp of nominally 1 V p-p, the period of which is the same as the plot duration of one line of data.

The Pen signal may be used to drop the plotter pen and start the plotter sweep. This signal is +5 V when not in Plot mode. When Plot is initiated, this signal drops to 0 V for the duration of each line of data. The signal goes to +5 V between each line of data to allow the recorder pen time to retrace.

3.43 Digital I/O

The 8200 has a complete digital interface: not only can digital data stored in memory be read out, but also the front panel switch positions may be sensed and/or programmed.

The data stored in memory is capable of being read via an asynchronous transfer, using Command and Flag bits. The rate at which data is transferred is completely controlled by the external device. Rates at which data is available varies from zero words per second to 3×10^6 words per second. Data is available at any rate within this band.

Words are presented at the interface in an 8-bit parallel structure.

All front panel functions, with the exception of display controls, power switch, and the external program selector switches, are fully software addressable, using a 16-bit parallel instruction. In addition, the front panel switch positions and/or the program instructions loaded into the unit may be read on the output lines. For details of the Program I/O and digital output structure, refer to Section V.

3.5 Operational Functions

The operation of the Model 8200 is basically concerned with the signals or events that determine the initiation and termination of the sampling and recording of the input signals. The following subparagraphs describe the various signals and events and their interrelationships in the functional operation of the unit.

3.51 Sweep and Sweep Time

In the following discussions the terms "sweep" and "sweep time" are often used. The term "sweep" is used to designate the succession of samples taken on the input signal during a recording sequence. The term "sweep time" is used to designate the amount of time required to fill the memory with contiguous samples of the input signal. When this term is used, it is normally assumed that the entire sweep was accomplished at a single linear sample rate.

3.52 Arm, Trigger and End of Sweep Functions

The Arm, Trigger and End Of Sweep functions, together with an adjustable delay (associated with the Trigger event) control the sequence of events in the operation of the record cycle of the Model 8200. The effect of each of these functions or events on the sequence of events is dependent upon the mode of operation selected for the unit. This interdependence will be described below.

In all recording modes, an Arm function must precede a Trigger function. The unit cannot be triggered before it is armed.

The Arm function may be initiated manually via front panel pushbutton, externally via front panel input, or automatically via internal circuitry. These options are selectable at the front panel.

Once the unit has been armed, it can accept a trigger.

The Trigger function may also be initiated in the same manner as the Arm function. In addition, the unit may detect a Trigger from the combinational trigger capability in the plug-in.

3.53 Modes of Operation

The operational modes for the record sequence in the Model 8200 are determined by the record mode selected and the choice of the Single or Dual Time Base function. Two basic record modes are provided. They are called Delayed mode and Pretrigger mode. The time base function selection and the record mode selection provide four basic record configurations under the control of the Arm, Trigger, and EOS events described in the preceding paragraphs. These four record configurations are illustrated graphically in Figure 3.2.

Delayed Record Mode, Single Time Base

In the Delayed record mode with the single time base selected, the record cycle is initiated by the (delayed) Trigger, and it is ended at the End Of Sweep (EOS). This mode can be used in various ways depending on the setting of the Trigger delay. With the delay set to zero, a straightforward sweep mode with no delay is produced.

The Delayed sweep mode can be configured for "delayed sweep" operation by setting the trigger delay to a significant value. The delayed sweep mode of operation is used in situations where the only good trigger signal precedes the data to be recorded. In many cases the delay between the trigger and the desired information is greater than the optimum sweep time. In these cases the signal would not be recorded with sufficient resolution to be useful. By delaying the initiation of the sweep with the Trigger Delay and sampling the signal at a faster rate, the information can be recorded with good time resolution.

The use of a digital delay switch allows precise selection, in increments of ten sample intervals, of Trigger delay.

Pretrigger Mode, Single Time Base

Pretrigger recording is a unique feature of Biomation Waveform Recorders. Pretrigger recording allows the capture or recording of signals that are not known to be significant for recording until after the signal has occurred. Another good use of this mode is in cases where the only good trigger available <u>follows</u> the information of interest.

In the Delayed record mode the starting point for filling the memory with new information is <u>when</u> the trigger occurs, or later. In the Pretrigger record mode of operation the memory is continuously being updated after the unit has been Armed, and will discard information (from the "other end" of the memory) at the same rate. When the trigger occurs, the

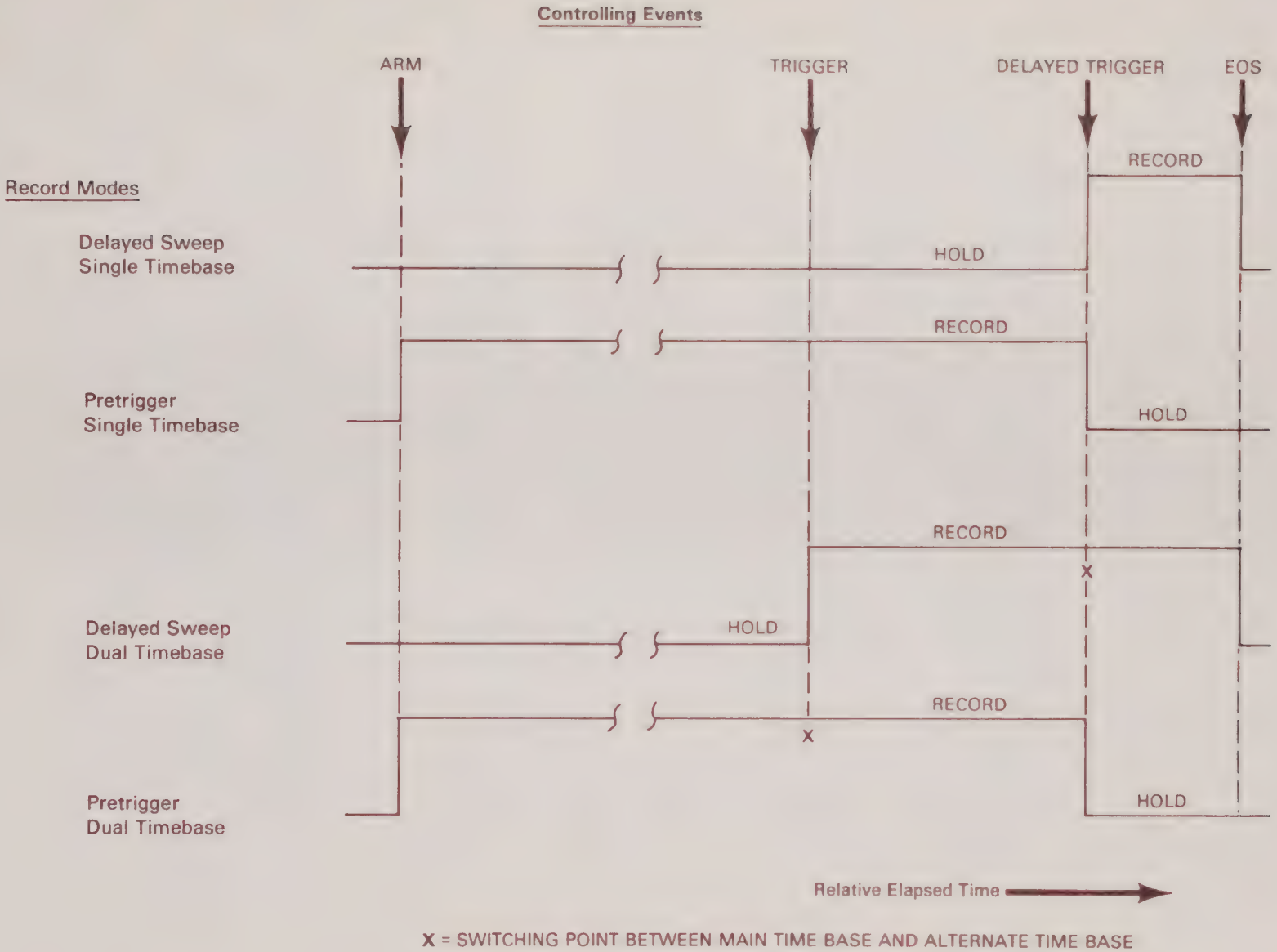


Figure 3.2 Model 8200 Recording Control Functions

recording function ceases after the selected Trigger delay time. If the Trigger delay is zero, the memory will contain the information for the signal that occurred for one complete sweep time prior to the trigger. The delay set on the Trigger delay in this mode will determine which portion of the signal in the memory occurred after the Trigger. Thus, any portion of the sweep time can be set to occur before or after the Trigger event in the Pretrigger record mode of operation by simply adjusting the Trigger delay setting.

Dual Time Base Operation

The Dual Time Base Operation of the Model 8200 permits the recording to begin at one sweep rate and conclude with a different sweep rate: i.e., sampling of the input signals in the Dual Time Base mode begins with sample intervals at one linear rate and switches to sample intervals at another linear rate for the conclusion of the recording period. The point at which the switching occurs is dependent upon the front panel control settings, and the record mode selected as described in the succeeding paragraphs. The Dual Time Base operation is useable for all combinations of sample intervals for each portion of the record sequence.

Delayed Sweep Mode, Dual Time Base

This mode permits the recording of an input signal with portions of the signal recorded at two independent rates. This is particularly useful in studying data that contains fast and slow rates. The point at which the record rate switches from the first sweep rate to the next is determined by the setting of the Trigger delay.

Thus, recording is initiated by the Trigger, the rate is changed by the Delayed Trigger, and the recording is terminated by EOS. Delayed sweep cannot be accommodated because the Trigger Delay is used for the record rate switching.

Pretrigger Mode, Dual Time Base

This mode is essentially the same as the Pretrigger record mode described above with the addition of the switching of the record rate by the Trigger. This mode is very convenient for recording at a slow rate a long period of time (but relatively few samples) prior to a trigger event, and then recording at a rapid rate (good time resolution) the signal occurring after the trigger event.

Thus, recording is initiated by the Arm, the rate is changed by the Trigger, and the recording is terminated by the delayed Trigger.

SECTION IV

OPERATION

4.1 Introduction

This section identifies and describes front panel controls, rear panel connections and typical operating procedures. Included are complete descriptions of front panel controls and their effective ranges, location and proper use of rear panel connectors, setup procedures prior to using the Model 8200 and step-by-step operating procedures for various modes of operation. A thorough understanding of this section is essential to the successful use of the instrument.

4.2 Front Panel Functions

4.21 Control Clusters

For the convenience of discussion, the front panel controls are divided into five groups of "control clusters." The clusters contain separate controls with related functions. In addition, the plug-in unit will be discussed separately. Figure 4.1 illustrates the plug-in, which contains the first cluster, the input controls and connectors.

Figure 4.2 illustrates the Mainframe control clusters as follows:

Display	Output
Time Base	Arm and Trigger

4.22 Digital Switches

Advantage has been gained through the digital nature of the unit by permitting the extensive use of digital control switches in lieu of the more common analog knob. This facilitates the readability, and, more importantly, the repeatability of the control settings. Use of this type of controls by the uninitiated does require some familiarization.

A unique type of switch is used both on the mainframe, and the Digital Detector plug-in. This is the leverwheel switch, which resembles a thumbwheel switch. However, a lever is used to change switch positions. This switch is very easy to operate and read. It has a definite detent feel.

4.23 Plug-in Functions for 8201-D Digital Module; refer to Figure 4.1

(1) Input Connectors

Eight connectors for input of as many digital signals. Input impedance switch selectable via switches (3).

Maximum input voltage.

50 Ω:+4 V
1 MΩ:±50 V

(2) PWR Connectors

Provides ±15 V and ground for powering active FET probes. For connector pin designations, refer to Digital Detector plug-in schematic in Section IX.

The receptacle is a LEMO RA 0.304 NYLU4,2. The The mating plug is a LEMO F 0.304 NYLU4.2. LEMO products are available from their warehouse in Berkeley, California.

NOTE: Maximum total current drain from all ten front panel probe power connectors shall be less than ±1.3 A.

(3) INPUT TERMINATIONS

50 Ω/GRD. Terminates respective input with a 50 Ω resistor to ground. May be used with active FET probes or 500 Ω X10 passive probes.

HIGH Z. Terminates respective input with 1 MΩ in parallel with 30 pF to ground. May be used with passive 10 MΩ X10 passive probes.

50 Ω/-2 V. Terminates respective input with a 50 Ω resistor in series with -2 V to ground. May be used directly with dedicated ECL driver circuitry requiring termination to -2 V.

(4) A/B

Allows selection of Threshold A or B reference for each channel.

(5), (6) THRESHOLD A, B

Permits selection of two different threshold levels so that two different logic families may be observed during one record sweep, or two thresholds may be selected for one family. Range of adjustment is ±2.975 V, in increments of 25 mV. Maximum amplitude hysteresis is 25 mV.

(7) SAMPLE/LATCH

In SAMPLE position, the unit stores the detected input logic level at the active clock edge for each clock cycle simultaneously on all input channels. Maximum channel-to-channel time skew of this clocked data is 1 nsec. Minimum pulse width always detected and recorded is one clock interval plus 1 nsec with 200 mV or more threshold voltage overdrive.

In the LATCH mode, pulses shorter than one clock interval occurring between active clock edges cause the input threshold detector to latch in a complementary state from that at the previous active clock edge. This changed state is stored in the memory at the next active clock edge. This latch acts as a detector of fast pulses and presents them in the time cells immediately following their actual occurrence. This input latch function may cause the latched data to be stored in one or two time cells following the detected pulse. Short pulses or data transitions occurring during adjacent clock time intervals may be merged in the recorded data. Minimum pulse width always detected in Latch mode is 3 nsec with 200 mV or more threshold voltage overdrive. Typical minimum is 2 nsec.

(8) COMBINATIONAL TRIGGER

Selecting "1" on any channel requires that the signal input to that channel transition be to a more positive (or less negative) level than the threshold setting, switches (5) or (6), for a ONE level to be detected.

Selecting "0" on any channel requires that the signal input to that channel transition be to a less positive (or more negative) level than the threshold setting, switches (5) or (6), for a ZERO level to be detected.

Selecting "X" causes the signal input to that channel to be ignored.

These switches are used to select a trigger event from any one of the channels, or to define a parallel combination of bits to be detected for the 8200 to be triggered.

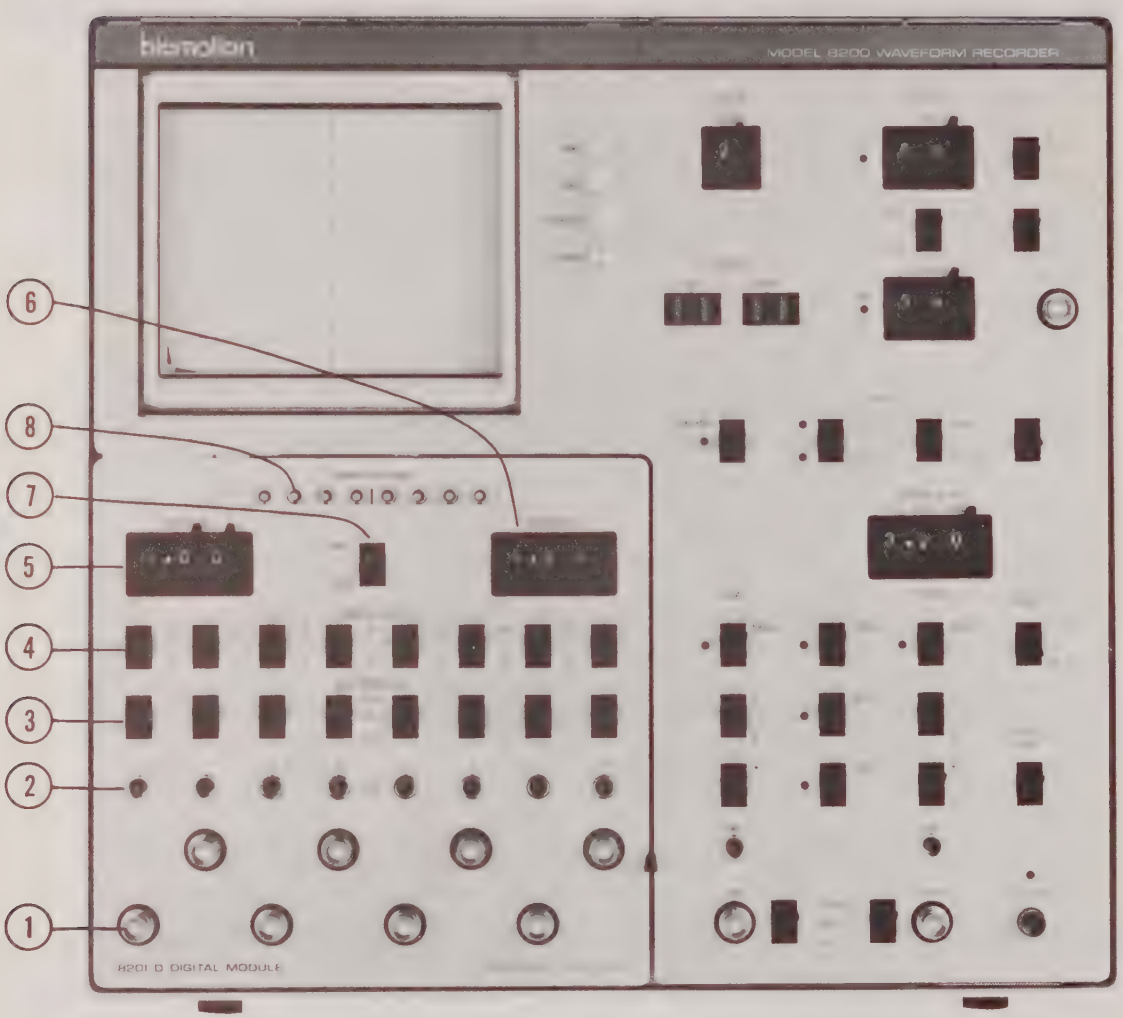


Figure 4.1 Plug-in Functions

4.24 Main Frame Functions; refer to Figure 4.2.

DISPLAY

(9) VERT

Controls vertical position of entire display field on internal CRT.

(10) HORIZ

Controls horizontal position of entire display field on internal CRT.

(11) INTENSITY

Controls intensity of CRT display.

(12) FOCUS

Controls focus of CRT display.

(13) DISPLAY EXPAND

Provides display expansion to give better visual resolution of displayed data. Expansion factors of X1, X2, X5, X10, X20, X50, X100. At expansion factors of X10 and greater, clock tics appear for marking each record sample interval.

Expansion is digital, so that the trace intensity remains constant.

(14), (15) LEFT, RIGHT CURSOR

Momentary switches move each cursor to the left and right. Switch is dual rate: slight movement of switch causes cursor to move slowly in the direction in which the switch was pushed. Pushing the switch all the way causes the cursor to move considerably faster.

A complete discussion of the operation and use of cursors and alphanumerics is given in Section 4.4.

TIME BASE

(16) MAIN

Permits selection of internal record sample intervals from 5 nsec to 5 sec in a 1-2-5 sequence. NO OP lamp indicates when a disallowed sample interval is selected.

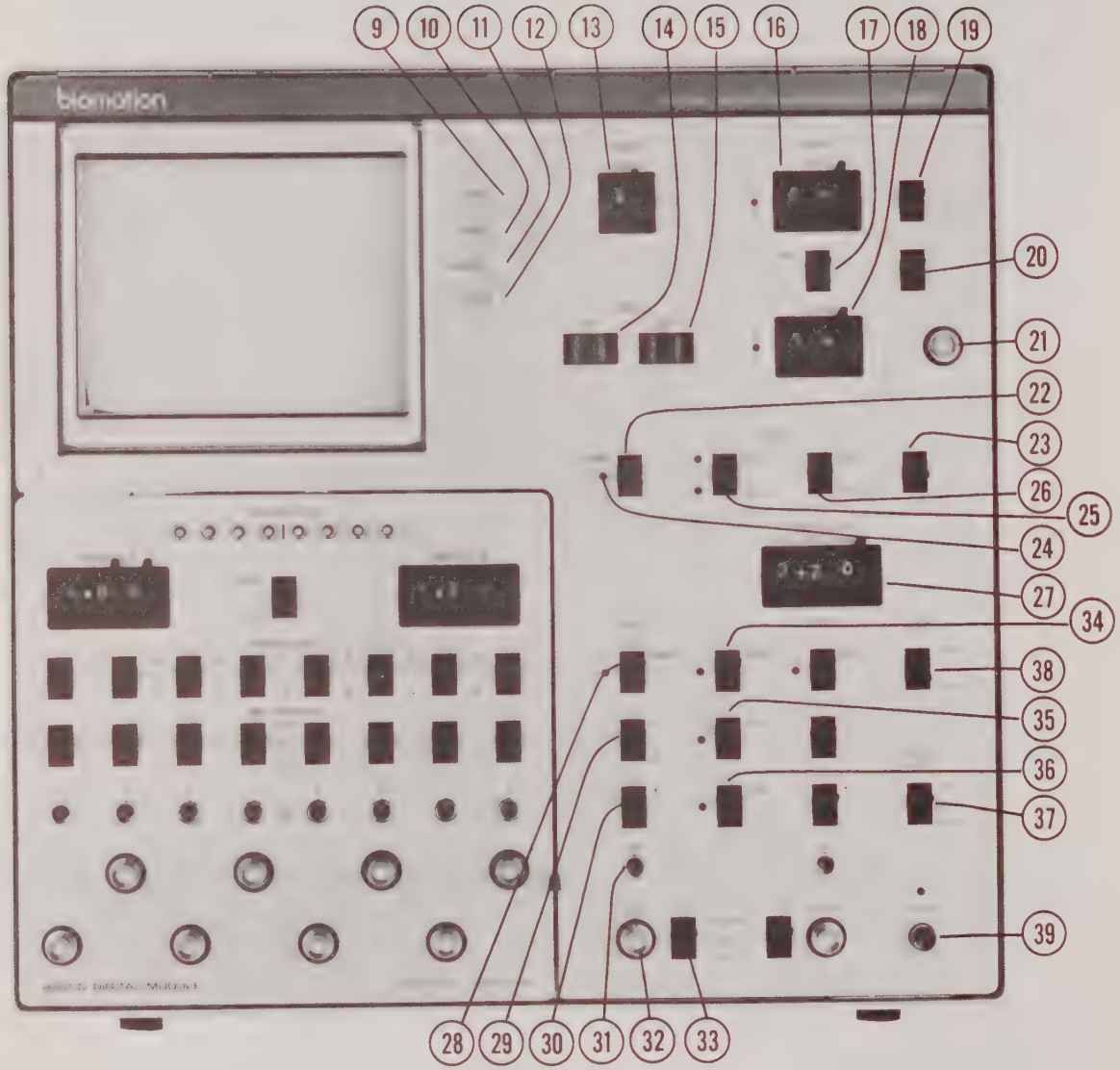


Figure 4.2 Main Frame Functions

This control also selects the main, or first time base for Dual Time Base recording.

(17) SINGLE/DUAL

In SINGLE position, allows recording with MAIN time base. In DUAL, allows recording in Dual Time Base Mode.

(18) ALTERNATE

Same as (16), but used to select the alternate, or second time base, for Dual Time Base recording.

(19) INT TB/EXT TB

Selects origin of time base to be used during record sweep. In either position, unit reverts to the Internal Time Base during display and output modes.

(20) ECL/TTL

Selects termination for external time base input; see (21).

(21) EXT TB IN

Allows input of an external clock for synchronous recording. Unit reverts to internal clock in display and output modes.

With switch (20) in ECL position, input termination is 50 Ω returned to -2 V. In TTL position, termination is 50 Ω to ground.

NOTE: There exists a fixed delay between the input data signals and the external clock input at the input threshold detectors, which is typically 12 nsec with the ECL clock input selected and 17 nsec with the TTL clock input selected.

OUTPUT

(22), (23) EXT PRG

Enables the user to manually initiate or cancel program control of the unit. BOTH switches must be pushed and held upward to initiate program control. The LED (24) will light when unit is under program control.

Likewise, to return to front panel control of the unit, BOTH switches must be held down at the same time. When under front panel control, the LED (24) will be off.

Using two switches for this function ensures that the act of switching between front panel and program control is a deliberate one. If the unit has been programmed, and front panel control is selected, ALL PROGRAM STEPS PREVIOUSLY LOADED WILL BE CANCELLED.

For the discussion of programming, refer to Section V.

(25) DIG OUT/PLOT

To initiate digital output after record mode is complete, and when unit is in display mode (usually referred to as "Edit" mode, where the data is visually examined before output), press switch up. The attendant LED (upper) will light. The display will blank out. Extract digital data as explained in Section V.

To truncate digital data, press the switch up once more. The LED will go out and display will return. To truncate digital output when in the AUTO DIG mode, press the switch up twice.

To initiate Plot mode, press switch down. The attendant LED (lower) will light. Display will blank momentarily and will return with a slow moving dot across the CRT at the rate selected internally (see Section VI for selectable Plot rates).

During Plot, turn down the INTENSITY control (11) to prevent damage to the CRT.

To truncate Plot mode, press the switch down once. The LED will go out, and display will return.

(26) NORMAL/AUTO DIG

When up (NORMAL), unit will record and will display memory contents, permitting an Edit function. Switch (25) may then be used.

When down (AUTO DIG), unit will record and will not display memory contents. Further recording will be inhibited until:

1. Memory contents are read;

   OR

2. Digital output is truncated via switch (25) or by program control.

ARM AND TRIGGER

(27) DELAY X1000 SAMPLE INTERVALS

Determines the time between detection of the Trigger (from Channel 1 internally or from an external event) and the actual triggering of the unit.

In the Delayed record mode, this control determines the number of sample intervals between Trigger and start of record. There exists a fixed minimum delay between the trigger event and the first data stored in memory of typically 8 clock intervals plus 70 nsec.

In the Pretrigger record mode, this control determines the number of sample intervals between Trigger and end of record.

Adjustment range is 0 to 9990 sample intervals, in increments of 10 sample intervals. The maximum selectable delay is approximately 5 memory lengths.

NOTE: For the following five items, both Arm and Trigger control functions are identical. Only the Arm group of items is described; the descriptions also apply to the Trigger group.

(28) ARM MANUAL

When in Single mode (see switch (36)), pressing this switch down arms the unit. Adjacent LED indicates when unit is ready for the Arm function.

In Delayed mode, the Arm function allows the unit to accept a Trigger function and begin recording.

In Pretrigger Mode, the Arm function starts the record sweep, allowing the (delayed) Trigger function to end the record sweep.

(29) A/B

When using the external Arm input (see (32)), this switch selects the threshold setting, THRESHOLD A (5) or THRESHOLD B (6), with respect to which the unit will detect an Arm event.

(30) +/-

Selects the positive or negative edge of the external Arm input signal for Arm detection.

The TRIGGER +/- switch, in addition to providing slope selection for the external trigger input, also allows negation of the COMBINATIONAL TRIGGER switches (8).

When TRIGGER +/- is in the + position, the unit will trigger when the selected combination of bits is detected. This is a combinational TRUE condition, and is an AND function of the COMBINATIONAL TRIGGER switches.

When TRIGGER +/- is in the - position, the unit will trigger ONLY after one or more of the selected bits changes from the detected pattern. This is a combinational FALSE condition, and is a NOR function of the COMBINATIONAL TRIGGER switches.

(31) PWR

Provides ±15 V and ground for powering active FET probes. For connector pin designations, refer to Front Panel schematic in Section IX.

The receptacle is a LEMO RA 0.304 NYLU4,2. The mating plug is a LEMO FO.304 NYLU4.2. LEMO products are available from their warehouse in Berkeley, California.

NOTE: Maximum total current drain from all ten front panel probe power connectors shall be less than ±500 mA.

(32) ARM

BNC input connector for external Arm signal. Input impedance is switch selectable via switch (33).

Maximum input voltage.

50 Ω:+4 V
1 MΩ:±50 V

(33) 50 Ω/GRD, HIGH Z, 50 Ω/-2 V

Provides input terminations for input (32).

50 Ω/GRD. Terminates input with a 50-Ω resistor to ground. May be used with an active FET probe or 500-Ω X10 passive probes.

HIGH Z. Terminates input with 1 MΩ in parallel with 30 pF to ground. May be used with passive 10 MΩ X10 passive probes.

50 Ω/-2 V. Terminates input with 50 Ω in series with -2 V to ground. May be used directly with dedicated ECL driver circuitry requiring termination to -2 V.

TRIGGER

NOTE: When powering up the unit, it will come up in any one of the following three modes.

(34) NORMAL

Pressing this switch down selects the Normal mode, where the Arm signal is automatically generated internally after a record sweep is completed. Adjacent LED

indicates mode selected. The Trigger signal must be input internally via the COMBINATIONAL TRIGGER or externally via the Trigger input. Not generally used with Pretrigger record mode.

(35) AUTO

Pressing this switch down selects the Auto mode, where both Arm and Trigger signals are internally generated automatically. Adjacent LED indicates mode selected.

This mode is generally used for setup only.

(36) SINGLE

Pressing this switch down selects the Single mode. In this mode, no automatic signals are generated. The Arm signal must be applied manually or externally, and the Trigger must be applied internally, manually, or externally for recording to take place.

This mode is ordinarily used for the Pretrigger record mode. It affords complete operator control over signal acquisition by the unit.

(37) EXT/INT

Selects the source of the Trigger signal. In EXT position, a signal applied to the external TRIGGER input will trigger the unit at the threshold selected by TRIGGER A/B, and on the rising or falling edge as selected by TRIGGER +/-.

In INT position, the unit derives its Trigger from the COMBINATIONAL TRIGGER switches (8).

(38) RECORD MODE DELAYED/PRE-TRIG

In the DELAYED position, the unit begins recording on the (delayed) Trigger and finishes recording when the memory is filled with new data (EOS).

In the PRE-TRIG position, the unit begins recording upon receipt of an Arm signal and finishes recording on the (delayed) Trigger.

(39) AC POWER

Latching pushbutton On-Off switch with LED to indicate power on.

4.3 Rear Panel Functions

The rear panel is illustrated in Figure 4.3.

The following four signal outputs are made available for those users who wish to use an external CRT display or oscilloscope to view the memory contents. These signals are all synchronized together. To ensure that the display is crisply defined, the vertical input bandwidth of the display device should be at least 1 MHz.

(1) OUT X

Repetitive triangle waveform for driving the X axis of an external CRT or scope. Period is 1 msec, and amplitude is 1 V p-p.

(2) OUT Y

Repetitive waveform of memory contents. For the 8200 with Digital plug-in, this signal is a stairstep, the first 8 msec of which contains alphanumeric information, and the second 8 msec of which contains memory information. Each line of data in memory is read out in 1 msec. The peak to peak deflection for the entire field of data plus alphanumerics is 1 V.

(3),(4) OUT Z, OUT $\overline{Z}$

Z and its complement, $\overline{Z}$, provide blanking for alphanumeric generation and retrace blanking. For Z, the blanking level is 0 V, while the unblank level is +3 V. For $\overline{Z}$, the reverse is true.

Unless these signals are used, the alphanumerics will not be generated on an external CRT.

The mechanics of the display and plot modes are as follows: each line of the display is made up of 2048 points. These points are scanned at a fixed rate. In the display mode, the scan rate is 2 MHz, resulting in each line of data being written on the CRT in a time period of 1 msec. The number of memory locations displayed is a function of the EXPAND control.

Thus, with an expansion factor of X1, all 2048 words are displayed across the CRT. As more expansion is selected, fewer words are displayed. For example, at an expansion of X50, only 40 memory words are distributed among the 2048 display locations. The exact words to be displayed are selected by use of the cursors, as explained in Section 4.4. This causes the rate at which the memory is scanned to be decreased.

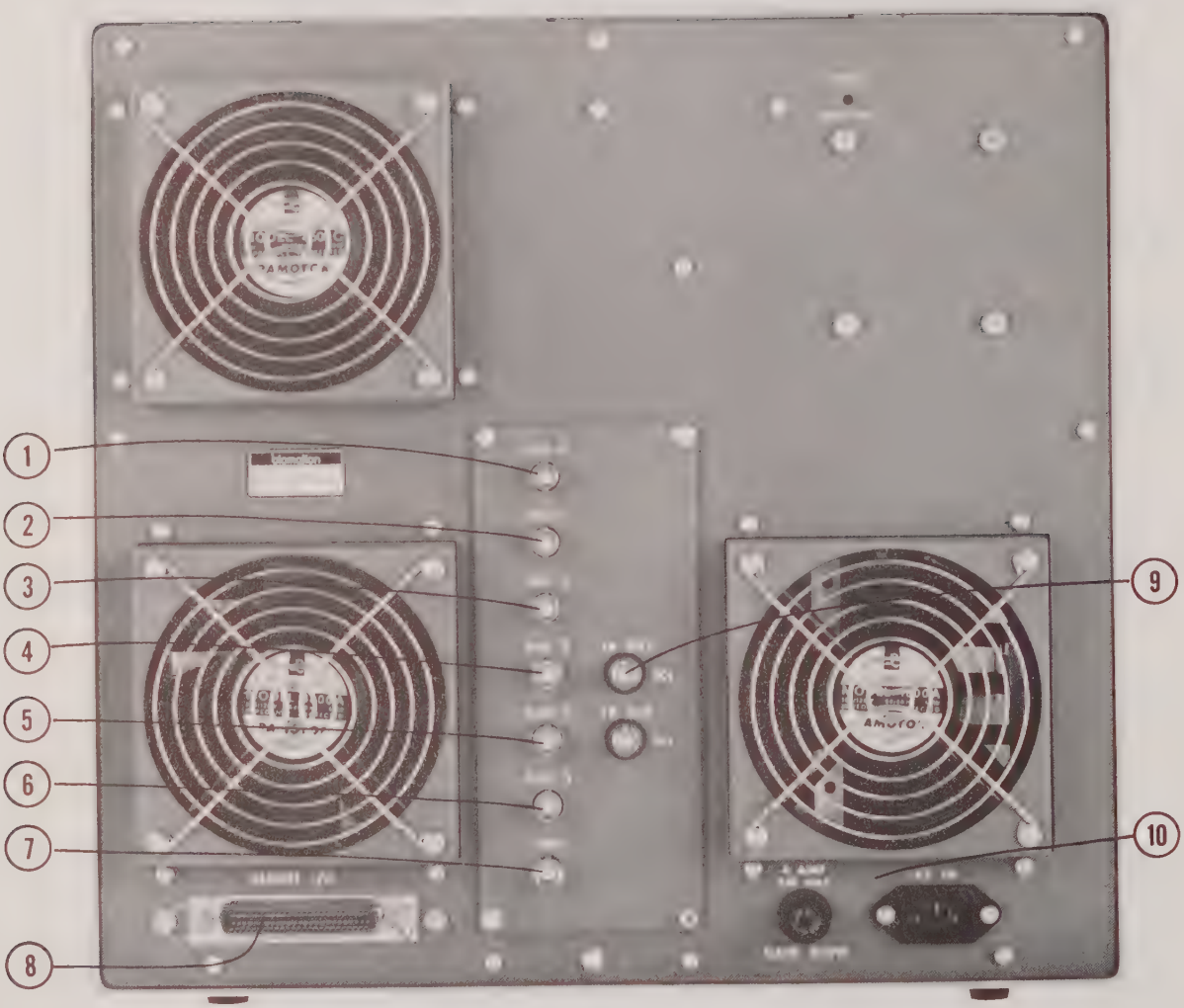


Figure 4.3 Rear Panel Functions

The plot output works in exactly the same fashion. The rate at which the 2048 display locations are scanned is switch selectable. The maximum scan rate in plot mode is 2 kHz and can be divided down by a factor of 2 or 4. Details of changing the plot rate are found in Section VI.

(5) PLOT X

Ramp output for plotter X axis. Period of ramp is controlled by the plot rate selected as explained in Section VI, 6.8.

(6) PLOT Y

Data output from memory. Numerics are not plotted. Unit plots each line of data, as depicted on CRT, when in plot mode. Select output rate as noted in Section VI.

Plot mode is initiated only when in display mode (not when recording), using switch (25).

Full field deflection is 1 V.

(7) PEN

Used to drop and pick up pen on recorder. Signal is 0 V during plot, +5 V otherwise. Polarity can be changed internally by strapping to give a +5 V level during plot. See Section VI, 6.9.

(8) REMOTE I/O

50 pin interface connector used for all I/O operations. For procedural details and pinouts, see Section V.

Mating plug is an Amphenol Ribbon 57-30500.

(9) TB OUT ECL

Two connectors are provided. This enables the user to connect two 8200s together for twice the data input capacity. Also, the user has access to the internal Time Base used for recording.

The proper procedure for operating two units on the Time Base of one is as follows: Use of any inter-connection scheme other than the one noted will cause time base errors in the recorded data.

1. Connect a BNC coax cable from one of the TB OUT connectors of unit 1 to the EXT TB IN connector (21) of unit 1.

2. Connect a BNC coax cable from the other TB OUT of unit 1 to the EXT of unit 2. Make sure that these two cables are exactly the same length.

3. Select EXT TB (19) and ECL (20) on both units.

4. Select the time base desired for recording on switch (16) of unit 1.

(10) AC LINE, Fuse, AC IN

AC LINE selects the proper line voltage on which the unit will be used. Use a small screwdriver to move the switch. Disconnect power, and change fuse, before changing switch.

For 115-V operation, use an AGC 4-A fuse, and for 230-V operation, use an AGC 2-A unit.

The cord supplied with the unit mates with AC IN.

4.4 Initial Operation

This section describes the steps necessary to record and display a known signal with the Model 8200. The operation of the cursors and alphanumerics are also covered.

4.41 Setup

Before connecting the unit to line power, check the line voltage selector switch (AC LINE 10)) on the rear panel to ensure that it is set to the proper line voltage, and that the proper size fuse is installed.

Power up the 8200 and allow time for the CRT to come on, usually a minute or less. Obtain a pulse generator capable of driving 50 Ω.

Set the controls of the pulse generator as follows:

Pulse amplitude	0 to +2 V
Pulse width	200 µsec
Pulse repetition rate	approximately 500 µsec

Set the controls of the 8200 as follows. Refer to Figure 4.1 and 4.2:

(4)	A/B	A
(5)	THRESHOLD A	+1.00
(7)	SAMPLE/LATCH	SAMPLE
(8)	COMBINATIONAL TRIGGER	First switch in "1" position; all others "X."
(9), (10), (11), (12)		As required to produce a centered and sharp display.
(13)	EXPAND	1
(14), (15)	CURSOR	To be covered below.
(16)	MAIN TIME BASE	1 μsec
(17)	SINGLE/DUAL	SINGLE
(19)	INT TB/EXT TB	INT TB
(22), (23)	EXT PROG	Press down, so that LED (24) is OFF.
(25)	DIG OUT/PLOT	Both LEDs OFF.
(26)	NORMAL/AUTO DIG	NORMAL
(27)	DELAY X1000 SAMPLE INTERVALS	0.00
	TRIGGER A/B	A
	TRIGGER +/-	+
(36)	SINGLE	Press, so that adjacent LED is ON.
(37)	EXT/INT	INT
(38)	DELAYED/PRETRIG	DELAYED

Connect the pulse generator to the Channel 1 input connector. Press ARM MANUAL (28) down. A display similar to that shown in Figure 4.4 should be on the CRT.

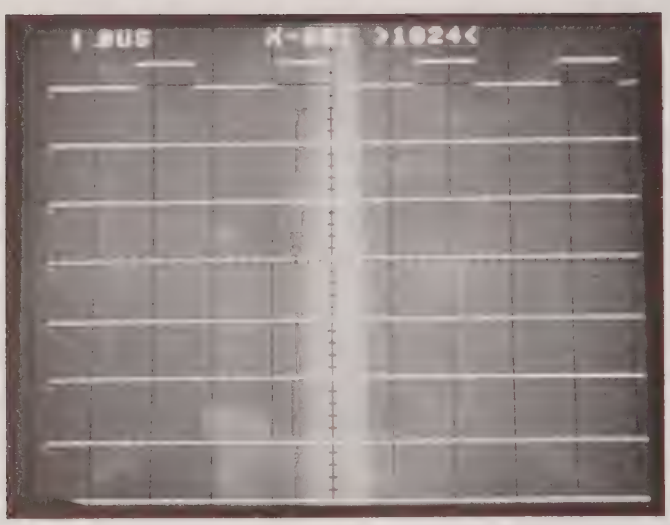


Figure 4.4. Scope Photo Showing Alphanumerics and Cursors

4.42 Cursor Operation

In Figure 4.4, the aids to visual analysis of the recorded data are evident: alphanumerics and cursors. Expansion is X1, showing 2048 sample intervals per line.

The first legend, 1.0 µsec, signifies that the data displayed was recorded at a sample interval of 1 µsec. Thus, one sweep represents a picture in time of 2.048 msec. This time period is measured with respect to, and starts with, the detected trigger event on Channel 1. Each division on the CRT equals approximately 200 µsec.

The second legend, X-001, indicates that the expansion factor is X1.

The third legend, >1024< , indicates that the cursors are 1024 memory words apart. To initialize the cursors, proceed as follows:

1. Hold LEFT CURSOR (14) full to the left until the small negative blip is at the left edge of the CRT, as shown in Figure 4.4. Let (14) go.

2. Move RIGHT CURSOR (15) to the left or right, depending on where the right cursor is. Note that each cursor switch has two speeds: a slight movement causes the cursor to move slowly, while the full over position causes much more rapid movement of the cursor.

3. Note that, while the right cursor is moving back and forth on the CRT, the third legend changes. This number marks the distance between cursors.

4. The left cursor is now at memory location zero. Place the right cursor at memory location 1024, and leave it there.

When using expansion, remember that the expanded data is always justified at the left edge of the CRT. In other words, the left cursor, regardless of where it is placed with X1 expansion, will ALWAYS be replaced to the left edge of the CRT for expansions of X2 and greater.

Change EXPAND (13) to 50. The CRT will look like Figure 4.5.

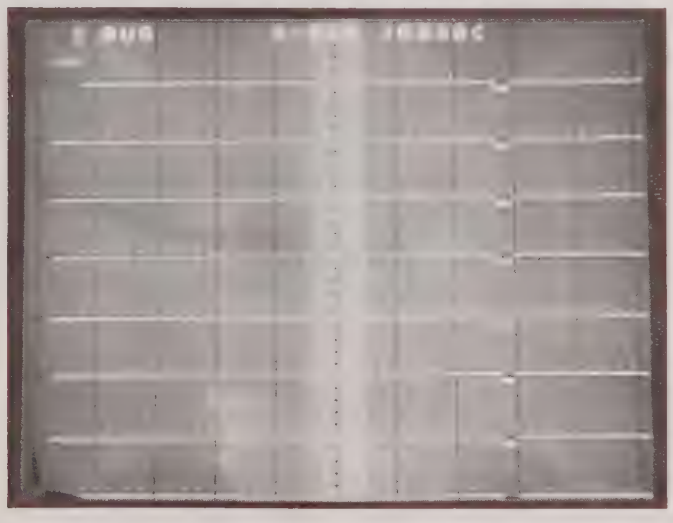


Figure 4.5. Display Expansion X50.

Using LEFT CURSOR (14), move the left cursor to within 30 sample intervals of the right cursor. The CRT will now look exactly like Figure 4.5. Note the expansion factor on the CRT. Also note the tics that appear to mark each sample interval. These tics appear at expansions of X10 and greater.

One more example of cursor operation will be given. Make the following control changes:

(13)	EXPAND	1
(16)	MAIN TIME BASE	2 µsec
(17)	SINGLE/DUAL	DUAL
(18)	ALTERNATE TIME BASE	5 µsec
(26)	DELAY X1000 SAMPLE INTERVALS	1.10

Press ARM MANUAL (28) down. The CRT will look like Figure 4.6. This is the Delayed, Dual Time Base record mode. The recording begins with the Main Time Base, and changes to the Alternate Time Base 1100 sample intervals after Trigger.

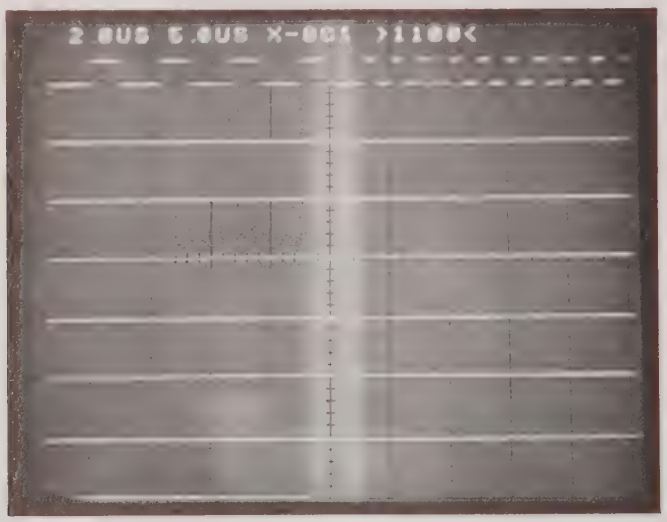


Figure 4.6. Dual Time Base

Place the left cursor at memory location zero, and the right cursor at location 1100 (the Time Base switch point). Expand to 5. Move the left cursor to within 250 sample intervals of the right cursor. The CRT will look like Figure 4.7.

Figure 4.7. Expansion X5, Dual Time Base

The right cursor marks the Time Base switch point, and the left cursor is at the left side of the CRT. Note the two different pulse widths. Since the Main Time Base is 2.5 times faster than the Alternate Time Base, the pulse to the left of the cursor is 2.5 times wider than the pulse to the right of the cursor.

By using the technique outlined here, you will find that the operation and use of the cursors and CRT numerics is quite simple. As you become more familiar with them, you can develop your own shortcuts with the cursors.

Note that the cursors may be placed 2038 sample intervals apart. In this case, the left cursor occupies memory location zero, the right cursor occupies memory location 2039, and the balance of the memory (8 sample intervals) is displayed to the right of the right cursor. These 8 intervals may be seen by expanding the display and positioning both cursors to the extreme right end of the CRT.

SECTION V

DIGITAL CONTROL INTERFACE

5.1 Introduction

The digital interface of the Model 8200 provides a versatile and comprehensive means to monitor and/or control the entire unit as well as to read out the recorded data in the unit's memory. This interface also contains the control, isolation and timing circuitry for direct parallel connection on a timeshare "bus" of a digital computer along with other like or similar devices. Conversely, the interface can be readily set to simply output the recorded data to a dedicated mass storage device under the control of rudimentary external interface circuitry.

Essentially all but a very few of the front panel control functions on the 8200 can be programmed via the unit's digital interface. Or, the front panel controls can be left operative and their settings can be read out through the unit's digital interface. In either case, the unit's operational status (e.g., recording, displaying, ready for trigger, etc.) and the recorded data can be read out through this interface.

These digital input and output functions are efficiently effected by a bit-parallel word-serial data exchange. That is, the digital functions are executed by successive digital "words" made up of a number of parallel bits. This data exchange is asynchronously controlled by two signals: The Flag (FLG) output bit and the Command (CMD) input in a "handshake", closed loop control which ensures that neither the data read nor write function will occur when the data is changing.

The digital interface is readily configured for a specific type of bus structure by a set of internal Logic Definition (LD) switches. These internal switches permit the user or systems designer to select the logic definition (i.e., positive true or negative true) in the input and output data bits. Also included with these LD switches are three switches for assigning the "address" of the unit. Thus, when a number of units (up to eight) are connected in parallel on a digital "bus", each can be individually controlled or read out.

5.2 Data Description

In order to understand the operation of the interface, it is essential that the functions that affect the data contents be understood. The following statements are intended to aid in that necessary understanding. It is, however, recommended that a thorough familiarity with the Model 8200 be gained prior to attempting the task of interfacing the unit with another device through the digital interface.

As mentioned in the Introduction above, the front panel controls can be either read as to their settings or these same functions can be programmed to any of their possible settings through the digital interface. This programming function does not, however, actually cause the front panel controls to change their physical settings. Rather, the programming instructions, when correctly input and executed, cause the unit to ignore the front panel control settings and act on the data received via the digital input data.

In order for the Model 8200 to accept any digital control input data to change the front panel control settings, two momentary front panel switches (EXT PRG) must be manually lifted such that both are held up at the same time. A front panel LED indicator will light indicating that the unit has been put under program control. A status bit in the status output data word will also be set so that the digital controller can also ascertain this information. Note that whether or not the front panel functions are manual or programmed, the status and stored data can be read out via the digital interface. Once under program control, the unit can be returned to manual front panel control simply by manually pushing both of the Ext Prg switches in the opposite direction (down).

This manual or programmed control capability is readily implemented in the unit because all of this control information, whether from the front panel switches or from the program data is stored in registers in the Model 8200. When the unit is under manual control, these registers are periodically updated with the front panel switch position information every sixteen milliseconds. When the unit is placed under external program control, this updating will cease. However, the data in these registers will not change until new data is input via the digital interface. Further, the read instructions for this control information do not actually read out the front panel switch positions. Rather, these instructions read out the information in the control registers. Thus, the read out data will indicate the actual control settings at all times whether set manually or via the program inputs.

The signal input section of the Model 8200 is a plug-in unit. The digital interface does provide program control for a number of the functions on this plug-in. The read and write control words for each plug-in are listed separately in the foregoing description.

5.3 Connector Definitions

The 50-pin rear panel connector provides the physical interface for digital output and control. The connector is an Amphenol Micro-Ribbon 57-0500. The mating connector is an Amphenol part number 57-30500.

The pin assignments for the digital interface are listed in the following table:

PIN #	MNEMONIC	DESCRIPTION
1	DO-8	MSB or Ch 8
2	DO-7	
3	DO-6	
4	DO-5	Output Data
5	DO-4	
6	DO-3	
7	DO-2	
8	DO-1	LSB or Ch 1
9	CMD	Input "Command"
10	AD-2	
11	AD-1	Input "Address"
12	AD-0	
13	OC-5	MSB
14	OC-4	
15	OC-3	Input "Op-code"
16	OC-2	
17	OC-1	LSB
18	DI-8	MSB
19	DI-7	
20	DI-6	
21	DI-5	Input Data
22	DI-4	
23	DI-3	
24	DI-2	
25	DI-1	LSB
26	FLG	Output "Flag"
27-49	GND	Signal Ground
50	+5V	+5 volts dc

5.4 Signal Specifications

This section describes the electrical and timing characteristics of the input and output signals for digital output and control of the Model 8200.

Inputs:

The inputs are comprised of 16 input connections (Input Data and Op-code) and the command control line (CMD). Each of these lines accepts standard TTL digital signals (2.4 to 5.0 V high, 0 to 0.4 V low) and presents a load approximating that of one and one-half TTL gates, i.e., each input line requires a nominal current sink of 2 mA to input a "low". The inputs can be positive or negative true (Pos or Neg Logic), depending upon the settings of the internal Logic Definition (LD) switches - see description below. The CMD input can be set for positive or negative true independently from the Input Data plus Op-code field.

Outputs:

The outputs are comprised of eight output connections (Output Data) and the flag control line (FLG). The FLG output is a supervisory data exchange bit used in conjunction with the CMD input. The output lines are only active when the unit is correctly "addressed." That is, the outputs do not present any signal nor place any load on the output lines unless the code on the input Address lines (AD-0, AD-1, AD-2) corresponds to the code selected on the appropriate internal LD switches - see description below. Each of the output lines is capable of driving up to 30 standard TTL loads (maximum fan-out = 30). The outputs will be positive or negative true (Pos or Neg logic), depending upon the settings of the internal LD switches - see description below. The FLG output can be set for positive or negative true independent from the Output Data field

Logic Definition (LD) Switches:

The versatility of the interface is considerably enhanced by a set of internal switches with which the digital input and outputs can be set to be either positive or negative true (Pos or Neg logic) and to assign a unique (one-in-eight) address to the unit. These switches are comprised of seven SPST switches in a single dual-inline-package (DIP) located on the Remote I/O circuit board. The Remote I/O circuit

board is accessible on the right side of the unit (as viewed from the front). The right sidecover of the unit must be removed in order to set the LD switches. The switches are quite small but easily set with the tip of a pencil or similar pointer. The LD switches are ON/OFF devices and the function for each one is marked on the circuit board as follows from left to right (as viewed with the connector away from the viewer):

1.	Flag	(FLG)
2.	Data Out	(DO-1/DO-8)
3.	Command	(CMD)
4.	Data In + Op-code	(D1-1/D1-8 + OC-1/OC-5)
5.	Address 0	(AD-0)
6.	Address 1	(AD-1)
7.	Address 2	(AD-2)

Setting the LD switch to "on" defines a positive logic convention, i.e., a "one" is high. Setting an Address LD switch "on" assigns a logic "one" (using a positive logic convention).

5.5 Control Timing

All digital inputs and outputs from the Model 8200 are regulated by two control signals: the output flag (FLG) signal and the input command (CMD) signal. The FLG output signal indicates the output data status of the Model 8200 and acknowledges the acceptance of input data. The CMD input signal initiates the data exchange function. This is sometimes referred to as "handshake" data exchange control.

In the following discussion, defining the FLG and CMD signals and their interrelationships, binary logic notation will be used, i.e., binary 0 (zero) and 1 (one) will be used to define the signals. These binary values are positive. The Flag and Command signals will be present only when the unit is properly "addressed" as described above. The following statements define the logic levels, timing and transitions for the FLG and CMD signals as well as their interrelationships and timing with respect to the input and output data.

1. Flag (FLG) level 1:

   When the FLG signal is a binary 1, any output data requested is available to be read on the output lines (assuming that the proper request data code is present on the input data and Op-code lines). The FLG equals one state also indicates that the unit is ready for the next data command.

2. Command (CMD) 0 to 1 transition:

   Accepted by the unit only when FLG is a 1. This CMD transition initiates a data transfer cycle. Any input data or Op-code accompanying the CMD should be applied and settled on the input lines prior to this CMD transition. If output data is being requested, the CMD transition will initiate the fetch of the data.

3. FLG 1 to 0 transition:

   The FLG signal will transition from a 1 to a 0 state in response to a correctly input 0 to 1 CMD transition. The FLG signal will remain 0 during the time it takes the unit to accept or execute the input instruction.

4. FLG 0 to 1 transition:

   The 0 to 1 transition of the FLG signal denotes that the input data instruction has been executed and that any output data can be read. Any output data requested will be applied to the output data lines prior to this transition. This output data will be held as long as the input instruction data (which enables or "gates" the appropriate output data) is maintained and the CMD is held at a 1. If no output data is required, the input data may be changed.

5. Minimum pulse width:

   The minimum "dwell" time in either the binary 1 or 0 state for the CMD signal is 100 nsec. A narrower pulse width may result in failure of the unit to recognize the signal. Similarly, the FLG output signal will not be produced with binary 1 or 0 pulses of less than 100 nsec duration.

5.6 Data Signal Considerations

The Model 8200 is designed to facilitate rapid digital data transfer. The TTL level data signals are arranged for a maximum data transfer word rate of about 3 mHz. This output rate is asynchronous with respect to the 8200 at a rate determined by the using (taking) device. Data can be transferred to or from the unit at virtually any rate up to the maximum word rate.

The unit's digital interface signals are essentially TTL level square-wave type signals that, particularly at high word rates, are subject to cross-talk and ringing problems unless good design practices are used with the data cable, line terminations, etc. When proper terminations

and twisted pair cables are used, data can normally be transferred at data word rates of 0.5 mHz and above over short distances of about 10 to 20 feet without problems. Longer distances are feasible at lower word rates with the same techniques and some low pass filtering of the signals.

5.7 Memory Data Output Controls and Functions

In addition to the External Programming (Ext Prg) controls previously described, there are two more front panel controls that can be used as a function of the digital interface. These two controls are to be used to facilitate the output of the recorded data in the 8200. The function of these two controls may also be programmed through the interface when the unit is under remote program control. These two controls are the Normal/Auto Digital (NORMAL/AUTO DIG) selector switch and the Digital Output (DIG OUT) momentary switch.

The Normal/Auto Dig Switch provides the following selection of functions:

NORMAL: The selection of this function allows the contents of the memory to be read out on demand at any time that the unit is not recording. At the end of recording, the unit will begin to repetitively reproduce the memory contents and generate a display on the CRT. With NORMAL selected (or programmed), a subsequent momentary operation of the DIG OUT switch will stop the display function and initiate the data output. Or the digital output can be initiated via proper digital instruction inputs described in succeeding paragraphs). Once initiated, the data can be strobed out of the unit by 2048 CMD/FLG "Handshakes" as described above. This data output can be terminated simply by repeating the DIG OUT momentary function prior to a complete "dump". The unit will also automatically terminate the digital output as soon as all of the memory contents have been read out. This read function is nondestructive and the memory contents may be repetitively output in this manner simply by reissuing the DIG OUT function after each complete memory "dump".

AUTO DIG: The selection of this function automatically initiates the recorded data output transfer immediately after the end of recording. This eliminates the need to use the DIG OUT function and provides the most rapid cycle for recording and outputing the data. Once the 2048 words of data are strobed out of the unit by FLG/CMD "Handshakes", the unit will automatically revert to the repetitive display operation. The data transfer can be terminated prior to a complete memory "dump" simply by selecting (or programming) the NORMAL output function. Again, this data transfer is nondestructive.

In order to effect the output of the recorded digital data, the following steps must be observed:

1. The unit must be correctly "addressed": i.e., the three address input lines (AD-0/AD-2) must be held in the proper high or low states as defined by the LD switches (previously described).

2. The Read Memory Op-code (described under programming codes) must be applied to the Op-code input lines (see next major section for simplified data output).

3. The data output must be initiated (either on demand in NORMAL output or automatically when AUTO DIG is selected - see description above).

4. The data must be strobed through the interface a-word-at-a-time with FLG/CMD "Handshakes" (see preceding description).

With the unit properly addressed and the Read Memory Op-code applied, the initiation of the data output (in NORMAL or AUTO DIG) will cause a transition of the Flag (FLG) to a one state signifying that the first word in the memory is present on the data output lines (DO-1/DO-8) and can be read. (A bit in the output data from a Read Status Op-code will also indicate that the data transfer has been initiated - see description under programming codes).

5.8 Simplified Memory Read Out Configuration

The digital interface of the Model 8200 can be easily configured to simply output the data in the memory without resorting to complex program control. To accomplish this, proceed as follows:

1. With no connection made to the address input lines (AD-0/AD-2), these inputs will "float" high. Therefore, the unit is readily "self-addressed" by simply setting the three internal address definition switches (see previous LD switch section) to "all ones", i.e., all "ON".

2. The Read Memory Op-code mentioned above can be permanently input to the unit by connecting pins 13 and 17 on the rear panel interface connector to Signal Ground (pins 27 through 49). Note: Be sure that positive logic is selected on the LD switches for the Op-code.

3. Now, whenever the output function is initiated (manually with the DIG OUT switch in NORMAL or automatically when AUTO DIG is selected), the data can be simply strobed out with the FLG/CMD signals. Alternatively, the FLG

output signal may be ignored at word rates below 1 MHz and the data strobed out with simply input pulses to the CMD input. These CMD pulses will determine the data output word rate.

5.9 Programming Data Codes

This section describes the digital input and output codes required to control and/or monitor the operation of the Model 8200 via the digital interface. All front panel functions can be set or monitored (write or read functions) except for the following:

1. Mainframe functions:

   Display controls, e.g., vert, focus, expand
   Display cursor controls
   EXT PRG switches
   AC Power Switch
   Arm and trigger input impedance switches

2. 8201-D Plug-in:

   Combination trigger switches
   Input impedance selection switches

The Op-codes and data codes to set or monitor all other front panel functions are listed in the following paragraphs. The following table lists all of the units Op-codes. Note that "Read" op-codes always result in data on the output data lines (DO-1 through DO-8) but require no input to the input data lines (D1-1 through D1-8). The converse is true for "Write" Op-codes. This permits operation on a half-duplex data bus; see discussion in a later section. Note also that in all "Read" op-codes OC-5 is a "zero" and all "write" OC-5 is a "one" with OC-4 through OC-1 remaining the same for both read and write of the same functions. Obviously, an op-code is either "read" or "write" depending on bit OC-5.

All op-codes except for Read/Write Status and Read/Write Memory have identical functions between read and write and identical output data codes (read) to input data codes (write). Therefore, the data codes listed in the following paragraphs (with these two exceptions) are given just once for both read and write.

OP-CODE TABLE

	OP-CODES	OC-5	OC-4	OC-3	OC-2	OC-1	DATA IN	DATA OUT
MAIN FRAME OP-CODES	READ STATUS	0	1	1	1	1		Yes
	WRITE STATUS	1	1	1	1	1	Yes	
	READ MEMORY	0	1	1	1	0		Yes
	WRITE MEMORY			NO OP				
	READ MAIN TIMEBASE	0	0	0	0	0		Yes
	WRITE MAIN TIMEBASE	1	0	0	0	0	Yes	
	READ ALT. TIMEBASE	0	0	0	0	1		Yes
	WRITE ALT. TIMEBASE	1	0	0	0	1	Yes	
	READ TRIG DLY I	0	0	0	1	0		Yes
	WRITE TRIG DLY I	1	0	0	1	0	Yes	
	READ TRIG DLY II	0	0	0	1	1		Yes
	WRITE TRIG DLY II	1	0	0	1	1	Yes	
	READ ARM/TRIG	0	0	1	0	0		Yes
	WRITE ARM/TRIG	1	0	1	0	0	Yes	
	READ OUTPUT MODE	0	0	1	0	1		Yes
	WRITE OUTPUT MODE	1	0	1	0	1	Yes	
8201-D PLUG-IN OP-CODES	READ THRES SELECT	0	1	0	0	0		Yes
	WRITE THRES SELECT	1	1	0	0	0	Yes	
	READ THRES AI	0	1	0	0	1		Yes
	WRITE THRES AI	1	1	0	0	1	Yes	
	READ THRES BI	0	1	0	1	0		Yes
	WRITE THRES BI	1	1	0	1	0	Yes	
	READ THRES A/B II	0	1	0	1	1		Yes
	WRITE THRES A/B II	1	1	0	1	1	Yes	

READ MEMORY (Requires previous initiation of DIG OUT mode)

	OC-5	OC-4	OC-3	OC-2	OC-1
Op-code:	0	1	1	1	0

Output data

DO-8	MSB or Ch 8	BINARY DATA FROM 2048 WORD MEMORY
DO-7		
DO-6		
DO-5		
DO-4		
DO-3		
DO-2		
DO-1	LSB or Ch 1	

WRITE MEMORY

No Op. This Op-code (11110) is illegal and will produce no action by the unit.

READ STATUS

	OC-5	OC-4	OC-3	OC-2	OC-1
Op-code:	0	1	1	1	1

Output Data:

DO-8	1 = Arm Ready
DO-7	1 = Trigger Ready
DO-6	1 - Recording in process
DO-5	1 - Memory data output in process
DO-4	Reserved
DO-3	Reserved
DO-2	1 - Delayed, 0 - Pretrigger, Record Mode Selection
DO-1	1 - EXT PRG switches set

WRITE STATUS

	OC-5	OC-4	OC-3	OC-2	OC-1
Op-code:	1	1	1	1	1

Input Data:

DI-8	1 - Arm
DI-7	1 - Trigger
DI-6	1 = Record Reset
DI-5	1 = DIG OUT reset
DI-4	Reserved
DI-3	Reserved
DI-2	1 = DIG OUT Initiate
DI-1	Reserved

MAIN TIMEBASE

	OC-4	OC-3	OC-2	OC-1
Op-code	0	0	0	0

I/O Data: Data Codes

Timebase Multiplier	nsec	µsec	msec	sec
DI/O-8	0	0	1	1
DI/O-7	0	1	0	1

Timebase Digit	0.1	0.2	0.5	1	2	5	10	20	50
DI/O-6	0	0	0	0	0	0	0	0	1
DI/O-5	0	0	0	0	1	1	1	1	0
DI/O-4	0	0	1	1	0	0	1	1	0
DI/O-3	0	1	0	1	0	1	0	1	0

DI/O-2 1 = Single Timebase, 0 = Dual Timebase

DI/O-1 1 = Internal Timebase, 0 = Ext. Timebase

ALT TIMEBASE

	OC-4	OC-3	OC-2	OC-1
Op-code:	0	0	0	1

I/O Data — Data Codes

Timebase Multiplier	nsec	µsec	msec	sec
DI/O-8	0	0	1	1
DI/O-7	0	1	0	1

Timebase Digit	0.1	0.2	0.5	1	2	5	10	20	50
DI/O-6	0	0	0	0	0	0	0	0	1
DI/O-5	0	0	0	0	1	1	1	1	0
DI/O-4	0	0	1	1	0	0	1	1	0
DI/O-3	0	1	0	1	0	1	0	1	0

DI/O-2 1 = Delay Record Mode, 0 = Pretrigger Recording

DI/O-1 1 = External ECL Clock Load

0 = External TTL Clock Load

TRIGGER DELAY I

	OC-4	OC-3	OC-2	OC-1					
Op-code:	0	0	1	0					
I/O Data:	Data Codes								
Delay MSD	0	1	2	3	4	5	6	7	8	9
DI/O-8	0	0	0	0	0	0	0	0	1	1
DI/O-7	0	0	0	0	1	1	1	1	0	0
DI/O-6	0	0	1	1	0	0	1	1	0	0
DI/O-5	0	1	0	1	0	1	0	1	0	1
Delay NSD	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
DI/O-4	0	0	0	0	0	0	0	0	1	1
DI/O-3	0	0	0	0	1	1	1	1	0	0
DI/O-2	0	0	1	1	0	0	1	1	0	0
DI/O-1	0	1	0	1	0	1	0	1	0	1

TRIGGER DELAY II

	OC-4	OC-3	OC-2	OC-1
Op-code:	0	0	1	1

I/O Data: Data Codes

Delay LSD	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09
DI/O-8	0	0	0	0	0	0	0	0	1	1
DI/O-7	0	0	0	0	1	1	1	1	0	0
DI/O-6	0	0	1	1	0	0	1	1	0	0
DI/O-5	0	1	0	1	0	1	0	1	0	1

Trigger:	NORMAL	AUTO	SINGLE
DI/O-4	1	0	0
DI/O-3	0	1	0
DI/O-2	0	0	1

DI/O-1 1 = External Trigger Source

0 = Internal Trigger Source

ARM/TRIGGER

	OC-4	OC-3	OC-2	OC-1
Op-Code:	0	1	0	0

DI/O-8 NO-OP

DI/O-7 1 = Arm Threshold Source A
0 = Arm Threshold Source B

DI/O-6 1 = Arm Slope +, 0 = Arm Slope -

DI/O-5 NO-OP

DI/O-4 1 = Trigger Threshold Source A
0 = Trigger Threshold Source B

DI/O-3 1 = Trigger Slope +, 0 = Trigger Slope -

DI/O-2 NO-OP

DI/O-1 NO-OP

OUTPUT MODE

	OC-4	OC-3	OC-2	OC-1
Op-code:	0	1	0	1

I/O Data:

DI/O-8, -7, -6, -5 NO-OP

DI/O-4 1 = NORMAL Output, 0 = AUTO DIG Output

DI/O-3 1 = DIG OUT

DI/O-2 1 = PLOT OUT

DI/O-1 NO-OP

5.10 8201-D Plug-In Data Codes

THRESHOLD SELECT

		OC-4	OC-3	OC-2	OC-1
Op-code:		1	0	0	0
I/O Data:		Data Codes			
Threshold Source		A	B		
DI/O-8	Chan 8	1	0		
DI/O-7	Chan 7	1	0		
DI/O-6	Chan 6	1	0		
DI/O-5	Chan 5	1	0		
DI/O-4	Chan 4	1	0		
DI/O-3	Chan 3	1	0		
DI/O-2	Chan 2	1	0		
DI/O-1	Chan 1	1	0		

THRESHOLD AI

	OC-4	OC-3	OC-2	OC-1
Op-code:	1	0	0	1

I/O Data: Data Codes

A Threshold Level MSD	+2 V	+1 V	+0 V	-0 V	-1 V	-2 V
DI/0-8	0	0	0	0	1	1
DI/0-7	0	0	1	1	0	0
DI/0-6	0	1	0	1	0	1

A Threshold Level NSD	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
DI/0-5	0	0	0	0	0	0	0	0	1	1
DI/0-4	0	0	0	0	1	1	1	1	0	0
DI/0-3	0	0	1	1	0	0	1	1	0	0
DI/0-2	0	1	0	1	0	1	0	1	0	1

DI/0-1 1 = SAMPLE 0 = LATCH

THRESHOLD BI

	OC-4	OC-3	OC-2	OC-1
Op-Code	1	0	1	0

I/O Data: Data Codes

B Threshold Level MSD	+2 V	+1 V	+0 V	-0 V	-1 V	-2 V
DI/O-8	0	0	0	0	1	1
DI/O-7	0	0	1	1	0	0
DI/O-6	0	1	0	1	0	1

B Threshold Level NSD	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
DI/O-5	0	0	0	0	0	0	0	0	1	1
DI/O-4	0	0	0	0	1	1	1	1	0	0
DI/O-3	0	0	1	1	0	0	1	1	0	0
DI/O-2	0	1	0	1	0	1	0	1	0	1

DI/O-1 NO-OP

THRESHOLD A/B II

	OC-4	OC-3	OC-2	OC-1
Op-code:	1	0	1	1

I/O Data: Data Codes

A Threshold Level LSD	0.000	0.025	0.050	0.075
DI/O-8	0	0	1	1
DI/O-7	0	1	0	1

B Threshold Level LSD	0.000	0.025	0.050	0.075
DI/O-6	0	0	1	1
DI/O-5	0	1	0	1

DI/O-4, -3, -2, -1 NO-OP

5.11 Parallel Operation

The digital interface of the Model 8200 is arranged to facilitate the operation of up to eight like or similar units on the same set of digital I/O lines. This is done simply by connecting each line or bit in the digital interface of all of the units in parallel with the respective line in the controlling device. Each of the units can then be separately controlled by supplying its unique address (as assigned on each unit) along with the desired digital instructions to that unit.

Parallel operation of the Model 8200 is aided by the use of so-called "tri-state" logic driving all of the unit's digital output lines. This type of logic presents essentially no load (or voltage) on the output lines when it has not been enabled by the specified "address" combination inputs. Thus, the output of paralleled units do not "fight" each other and no signal degradation is caused by the parallel connection. This is only true, of course, if all paralleled units have different assigned addresses. Identical addresses on two or more paralleled units will, of course, cause contention.

The Model 8200 may be paralleled with similar devices that do not have "tri-state" output but use the more common "open-collector" logic for their digital output lines providing the common load resistor for the open-collectors on each output line is returned to +5 V and the outputs of any of these units are arranged to "go high" when they are not "addressed".

5.12 Half Duplex Operation

The output data lines of the digital interface for the Model 8200 can be connected in parallel with the input data lines without affecting the operation of the unit. Examination of the op-codes reveals that no op-code requires both input and an output data. Thus, no contention or "lock-up" conditions exist within the unit. Therefore, this type of operation is feasible if the controlling device has the capability to use the same lines for inputs and output (i.e., half duplex data transmission) as a function of its normal operation.

SECTION VI

CALIBRATION PROCEDURE

6.0 Introduction

The following calibration procedure is intended to be used in recalibrating the internal circuits and display of the 8200. The entire instrument was calibrated before shipment and should not need any recalibration for at least six months or 1000 hours of operation.

NOTE: Before starting the calibration procedure, please read the procedure completely. Pay special attention to the NOTES and CAUTIONS as they make for a better understanding of the unit.

6.1 Required Test Equipment

No. Required	Description	Required Specifications and Accuracy
1	Digital Voltmeter	3-1/2 digits mV range
1	250-MHz Scope	BW $\geq$200 MHz
1	250-MHz Pulse Generator	P_o <3 nsec

6.2 Test Setup

All voltage measurements are made on the 8201-D plug-in module. P/S voltage measurements are taken at the top left corner of the 8201-D logic board.

The 8201-D plug-in module framework may be used as ground. However, the chassis of the 8200 may not be used as ground for any voltage measurements.

6.21 Display Adjustments

All adjustments are to be made with either a nonconductive or a completely insulated screwdriver as indicated.

Select the front panel controls to:

1. Source: INT TB
2. Single/Dual: SINGLE
3. Timebase Main: 5 nsec
4. Display Expand: X1
5. Output Normal/Auto Dig: NORMAL
6. Trigger Delay: 0.00
7. Record Mode: DELAYED
8. Trigger Source: INT CH 1
9. Trigger: AUTO, then SINGLE
10. Arm Termination: 50 Ω/GND
11. Trig Termination: 50 Ω/GND
12. Combinational Trigger: ALL X
13. Sample/Latch: LATCH

6.3 Power Supply Adjustments

> CAUTION
>
> USE AN INSULATED SCREWDRIVER AS EXPOSED COMPONENTS HAVE VOLTAGES INCOMPATIBLE WITH GROUND.

Remove top cover and both side covers. Supplies must be adjusted in the following order:

1. +5 VDC ±0.01 VDC. Adjust R48 through the adjustment port on the right side of the instrument.

   NOTE: The use of a strong light shone through the side of the power supply will facilitate location and adjustment of remaining power supply voltage potentiometers (pot).

2. +15 VDC ±0.01 VDC. Adjust R17 through the front adjustment port on the top of the unit. The pot is located slantwise to the inside and rear of the unit.

3. -15 VDC ±0.01 VDC. Adjust R33 through the adjustment port in the top center of the unit.

4. -5.20 VDC ±0.01 VDC. Adjust R8 through the front adjustment port on the top of the unit. The pot is directly beneath the adjustment port.

NOTE: See Figure 9.10, Steps 1, 2, and 3 for visual location of adjustments.

6.4 Horizontal "X" Adjustments

Adjustments are on the right side of the display control board. See Figure 9.9, Step 3.

1. Adjust R152 counterclockwise (CCW) until a gap appears 1/16 of the total trace width from the right edge of the display. See Figure 6.1.

2. Adjust R152 clockwise (CW) until this gap just disappears.

NOTE: A bright spot indicates overadjustment.

3. Adjust R153 CCW until a gap appears 1/8 of the total trace width from the right edge of the display. See Figure 6.1.

4. Adjust R153 CW until this gap just disappears.

5. Adjust R154 CW until a gap appears 1/4 of the total trace width from the right edge of the display. See Figure 6.1.

6. Adjust R154 CW until this gap just disappears.

7. Adjust R155 CCW until a gap appears 1/2 of the total trace width from the right edge of the display. See Figure 6.1.

8. Adjust R155 CW until this gap just disappears.

9. Adjust R110 for a 1 V p-p signal measured at the "X" out BNC on the rear panel. See Figure 6.2.

6.5 Vertical "Y" Adjustments

Adjustments are on the display control board on the left side of the board. See Figure 9.9, Step 3. Measurements are made at the "Y" out BNC on the rear panel.

1. Adjust R20 for 125 mV between the traces for Channel 7 and Channel 8. See Figure 6.3.

2. Adjust R57 for 125 mV between the traces for Channel 6 and Channel 7. See Figure 6.3.

3. Adjust R60 for 125 mV between the traces for Channel 4 and Channel 5. See Figure 6.4.

4. Adjust R170 for a 1 V p-p signal. See Figure 6.5.

NOTE: R170 adjusts the character positions only and may need to be slightly realigned to put the characters at the top of the display; see Step 3 of 6.72.

5. Input data on Channel 8. Adjust R62 for a data height of 50 mV on the trace for Channel 8. See Figure 6.6.

6.6 Intensity "Z" Adjustments

Adjustments are to the left of center on the display control board. See Figure 9.9, Step 3. Measurements are made at the "Z" out BNC on the rear panel.

NOTE: Scope may be synchronized to the SWP Ø TP.

1. Adjust R37 for a 2 V p-p data signal. See Figure 6.7.

2. Adjust R38 for a 2 V p-p character signal. See Figure 6.7.

6.7 Display Alignment (604 monitor)

The 604 monitors used for displaying the data have their own "X", "Y", and "Z" internal amplifiers.

The adjustment pots are located on the left side of the unit and are from rear to front "X", "Y", and "Z" respectively. See Figure 9.9, Step 2.

6.71 "X" Alignment of Display

Adjust the "X" amplifier to show a full-scale signal starting at the first graticule line on the left and ending at the 10th graticule line on the right.

6.72 "Y" Adjustment of Display

1. Position the Channel 8 trace slightly above the bottom graticule line of the display.

2. Adjust the "Y" amplifier to place the Channel 1 trace slightly above the next to the top graticule.

NOTE: Slight vertical position changes may have to be made to keep Channel 8 at the bottom graticule.

3. Adjust R170 to put the top of the characters slightly beneath the top graticule of the display.

NOTE: Slight vertical position changes may have to be made to keep the data positions at the graticules.

6.73 Trace Rotation

Adjust trace rotation through the rear panel so that the horizontal data sweeps line up parallel with the display's horizontal grid lines. See Figure 9.4, Step 1.

NOTE: Adjustment shaft is recessed from the rear panel.

6.74 Focus. Adjustable from front panel control.

6.75 Astigmatism and Geometry. Accessible from the top of the display.

WARNING

USE OF AN INSULATED SCREWDRIVER IS MANDATORY AS DISPLAY HAS VOLTAGES HIGH ENOUGH TO BE DANGEROUS.

6.8 Threshold Adjustment

See Figure 9.8, Step 2 (Mode Control) for adjustment locations. From the left side of the board the first four pots are for Threshold A and the next four pots are for Threshold B.

6.81 Connect the DVM probe to R18 on the threshold selector board. See Figure 9.8, Step 1. It is the first 1KΩ resistor to the right of the outside ribbon cable connector.

1. Verify that all settings of the Threshold A digitswitch work correctly.

2. Set all pots near the center of their adjustment range.

3. Select all Threshold "A/B" switches on the plug-in to "A".

4. Select -0.00 on the Threshold A digitswitch.

5. Adjust R60 for approximately -3.0 mVDC <-2.0 mV, >-4.0 mV.

6. Select +0.00 on the Threshold A digitswitch.

7. Adjust R59 for approximately +3.0 mVDC >2.0 mV, <4.0 mV.

NOTE: If either R60 or R59 cannot be adjusted to the correct voltage without being at the end of its range of adjustment, readjust R62 ±200 mV for the appropriate ±0.00 setting and readjust R60 and R59 as per Steps 4 through 12.

8. Select +2.975 on the Threshold A digitswitch.

9. Adjust R63 for +2.975 VDC ±0.005 VDC.

10. Select -2.975 on the Threshold A digitswitch.

11. Verify -2.975 VDC ±0.005 VDC.

12. Verify that all settings of the digitswitch read within one Least Significant Bit (LSB).

6.82 Connect the DVM probe to R19 on the threshold selector board. See Figure 9.8, Step 1. It is the second 1KΩ resistor to the right of the outside ribbon cable connector.

1. Verify that all settings of the Threshold B digitswitch work correctly.

2. Set the Threshold B pots near the center of their adjustment range. Refer to Step 2 of 6.81.

3. Select all Threshold "A/B" switches on the plug-in to "B".

4. Select -0.00 on the Threshold B digitswitch.

5. Adjust R65 for approximately 3.0 mVDC <-2.0 mVDC, >-4.0 mVDC.

6. Select +0.00 on the Threshold B digitswitch.

7. Adjust R64 for approximately +3.0 mVDC >+2.0 mVDC, <4.0 mVDC.

NOTE: If either R65 or R64 cannot be adjusted to the correct voltage without being at the end of its adjustment range, readjust R67 ±200 mV for the appropriate ±0.00 setting and readjust R65 and R64 as per Steps 4 through 12.

8. Select +2.975 on the Threshold B digitswitch.

9. Adjust R68 for +2.975 VDC ±0.005 VDC.

10. Select -2.975 on the Threshold B digitswitch.

11. Verify -2.975 VDC ±0.005 VDC.

12. Verify that all settings of the digitswitch read within one Least Significant Bit (LSB).

6.9 DC Balance 50 Ω/GND

6.91 Set Auto Trig mode.

1. Select all termination switches to 50 Ω/GND.

2. Measure the center conductor of each BNC input to GND. The result should be 50 Ω.

6.92 Select all Threshold A/B switches to "A".

1. Select +0.00 on the Threshold A digitswitch.

6.93 For each channel of the plug-in, there is a 100 K, 4-turn potentiometer. See Table 6.1 "50 Ω/GND" for individual channel reference part numbers.

1. Adjust the 100 K pot for a logic "0" on the display. See Figure 6.8, top trace, Channel 1.

6.94 Select -0.00 on the Threshold A digitswitch.

1. Adjust the 100 K pot for a logic "1". See Figure 6.8, second from top trace, Channel 2.

NOTE: Step 1 of either 6.93 or 6.94 will be unnecessary as the pot will be one way or the other.

6.95 Verify that the channel being adjusted switches from logic "0" to logic "1" and back as the threshold is switched from +0.00 to -0.00 and back.

6.96 Repeat this procedure for all eight channels. See Figure 6.8.

6.10 DC Balance High Z

6.101 Select all termination switches to High Z.

1. Measure the center conductor of each BNC input to GND. The result should be between 0.9 MΩ and 1.1 MΩ.

6.102 Select +0.00 on the Threshold A digitswitch.

6.103 For each channel of the plug-in, there is a 100 K, 4-turn potentiometer located in a row behind the input BNCs on the front panel. See Table 6.1 "High Z" for individual channel reference part numbers.

1. Adjust the 100 K pot for a logic "0" on the display.

6.104 Select -0.00 on the Threshold A digitswitch.

1. Adjust the 100 K pot for a logic "1".

NOTE: Step 1 of either 6.103 or 6.104 will be unnecessary as the pot will be one way or the other.

6.105 Verify that the channel being adjusted switches from logic "0" to logic "1" and back as the threshold is switched from +0.00 to -0.00 and back.

6.106 Repeat this procedure for all eight channels.

6.11 AC Balance

The AC balance is a capacitive coupling for the extremely fast glitch-catching capability.

Each channel has its own capacitor. See Table 6.1 for individual channel reference part numbers. See Figure 9.8, Step 1 for locations.

Set the pulse generator for a 6 nsec output pulse from 0 to +1.50 V $\pm$0.01 V. Measure the 6 nsec at the 1.0 VDC level.

NOTE: See Figure 6.9 for measurement requirements.

6.111 Select combinational trigger to all "0s".

6.112 Select Threshold "A" on all channels.

6.113 Select +1.50 on the Threshold A digitswitch.

6.114 Select Auto Trigger.

6.115 Set oscilloscope to: 0.5 V/div, 0.01 µsec/div on X10 expand.

1. Set the oscilloscope input to GND. Adjust vertical position of the trace to 2.6 div above center line. Set input to DC.

6.116 Connect the oscilloscope probe to the output of the 685 pin 7 at the 130 Ω termination resistor. See Figure 9.18, TP 3. See Table 1 for individual channel reference part numbers. Also see Figure 6.10.

1. Adjust the variable capacitor for maximum pulse width and amplitude from the 685. See Table 6.1 for reference designation numbers. Also see Figure 6.10.

6.117 Repeat 6.116 for each channel.

6.12 External Arm DC Balance 50 Ω/GND.

The external arm circuitry is adjustable only with the trigger delay board on an extender board, preferably with traces S10, S13, and S24 replaced with coaxial cable. Use C10, C13, and C24 as ground returns. See Figure 9.8, Step 3 (trigger delay board) for adjustment locations. See Table 6.2 for trigger reference designation numbers.

6.121 Use the setup procedure in 6.21.

1. Select 50 Ω/GND input termination.

2. Measure the center conductor of each BNC input to GND. The result should be 50 Ω.

6.122 Set the arm Threshold "A/B" switch to "A".

6.123 Set scope as per 6.115 and Step 1 of 6.115.

6.124 Probe the output of the 685 pin 7 at the 160 Ω resistor, reference number R3.

6.125 Select +0.00 on the Threshold A digitswitch.

1. Adjust the 100 KΩ resistor, reference number R103, for a logic "0" on the scope.

6.126 Select -0.00 on the Threshold A digitswitch.

1. Adjust the 100 KΩ resistor R103 for a logic "1" on the scope.

NOTE: Step 1 of either 6.125 or 6.126 will be unnecessary as the pot will be one way or the other.

6.127 Verify that the output will change states from a logic "0" to a logic "1" and back as the threshold is changed from +0.00 to -0.00 and back. There will probably be a lot of noise on the output signal. Adjust the 100 K pot for the best balance between the two states.

6.13 External Arm DC Balance, High Z

6.131 Select High Z termination on the external arm.

6.132 Measure the center conductor of each BNC input to GND. The result should be between 0.9 MΩ and 1.1 MΩ.

6.133 Select +0.00 on the Threshold A digitswitch.

1. Adjust the 100 K pot reference number for a logic "0" on the scope.

NOTE: The 100 K pot is located on the edge of the board nearest the connector fingers.

6.134 Select -0.00 on the Threshold A digitswitch.

1. Adjust the 100 K pot for a logic "1" on the scope.

NOTE: Step 1 of either 6.133 or 6.134 will be unnecessary as the pot will be one way or the other.

6.135 Verify that the output will change states from a logic "0" to logic "1" and back as the threshold is changed from +0.00 to -0.00 and back. There will probably be a lot of noise on the output signal. Adjust the 100 K pot for the best balance between the two states.

6.14 External Arm AC Balance

6.141 The AC balance is a capacitive compensation for the leading edge of a pulse.

6.142 Remove the scope probe.

6.143 Select 50 Ω/GND input termination.

6.144 Input a 5-msec pulse of 0 V to +1.500 V ±0.005 V.

6.145 Select +1.50 on the Threshold A digitswitch.

1. Adjust the capacitor C80 so that the unit will arm externally.

6.146 Select +1.525 on the Threshold A digitswitch.

1. Adjust the capacitor C80 so that the unit will not arm externally.

NOTE: This adjusts the input pulse for the best capacitive compensation on the leading edge.

6.15 External Trigger Input

6.151 Use trigger source: EXT. The external trigger input is adjusted in the same way as the external arm input. Only the adjusted components change. See Table 6.2 for the part reference number changes. See Figure 9.8, Step 3 (trigger delay board) for adjustment locations.

Table 6.1

CH	50 Ω/GND	HIGH Z	C	685 OUTPUT
1	R45E	R65	C23E	R23E
2	R22E	R66	C 3E	R51E
3	R45D	R67	R23D	R23D
4	R22D	R68	C 3D	R51D
5	R45B	R69	C23B	R23B
6	R22B	R70	C 3B	R51B
7	R45A	R71	C23A	R23A
8	R22A	R72	C 3A	R51A

Table 6.2

EXT INPUT	50 Ω/GND	HIGH Z	C	685 OUTPUT
Arm	R103	R134	C80	R3
Trig	R104	R135	C81	R10

SECTION VII

TECHNICAL DESCRIPTION

7.0 Introduction

Section VII is divided into two parts. The first part is the functional overview of operation. This description is oriented toward a specific flow of events. The object is to follow a definite function or control setting from initiation to completion and to identify the logic or data path in order of occurrence through block diagrams and flow charts.

The second part is the detailed circuit-by-circuit analysis of the circuitry involved in the 8200. It is presented in a board-by-board form, with references to means of interconnection, schematic location, circuit description, and philosophy of implementation. This section provides the fine details of operation.

7.1 System Overview

The 8200 is actually a system within an instrument. The control register board is the central point for commands to the corresponding machine functions. Either the front panel or the inputs from an external controller have access to the control register board. When the unit is in external program mode, the front panel inputs to the control register are disabled and the external inputs through the RI0 board are enabled to the control registers. When not in external program mode, the front panel inputs are enabled to the control registers. The timing generated through the RI0 board coordinates the transfer of information from the front panel to the control register. When in external program mode, the OP code, which is part of the command word, is decoded for addressing on the control register and the command pulse is used to develop the write pulse on the control register board. See Figure 7.1a.

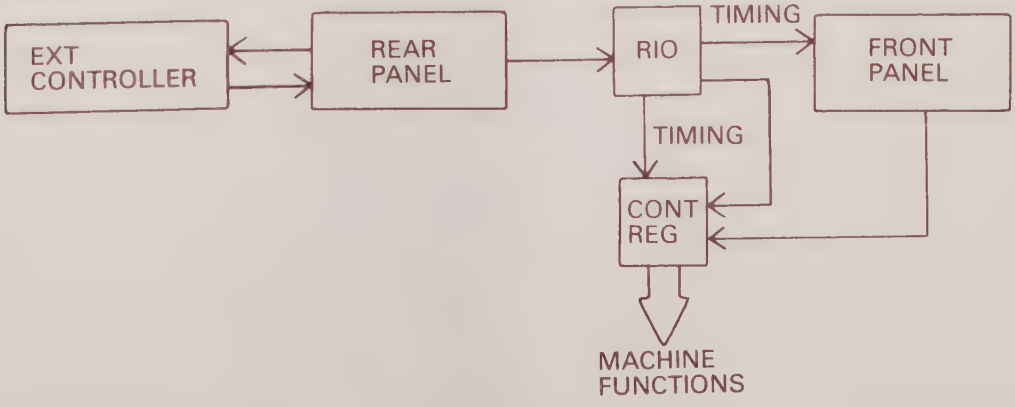


Figure 7.1a

7.11 Front Panel Controls

Refer to Figure 7.1b. All front panel selectable controls and settings are constantly updated and stored in flip-flops on the "control register" board. The condition of these flip-flops is what the control logic sees as direction.

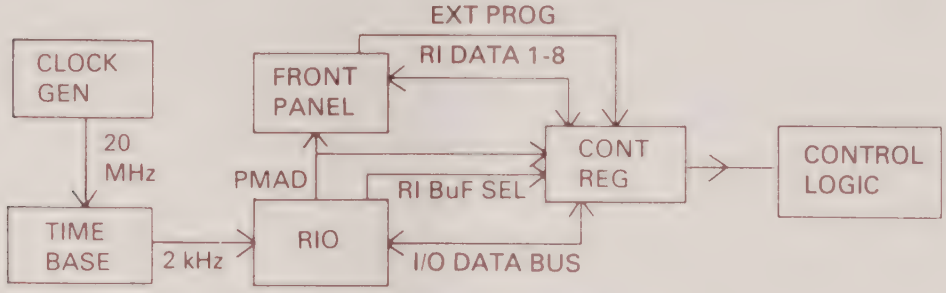


Figure 7.1b

All data (switch settings) are transferred to the control register via a time-shared bus. The timing for access to the bus (RI Data 1-8) is derived by 1 kHz driving a (74161) binary counter to supply PMAD 1, 2, 4, 8. See Figure 7.2, Timing Diagram. The PMAD lines provide specific timings and enables by means of a decimal decoder (7442 BCD to decimal). The same BCD to decimal conversion done on the control register board provides the receive synchronization of data.

BCD to decimal is used as enables to place a setting on the R1 data bus. The BCD to decimal on the control register is used as a clock to the flip-flops at the corresponding time.

NOTE: When in external program mode, the "Ext Prog" level disables the PMAD lines on the control register board eliminating front panel control of the 8200. Ext Prog enable "R1 BUF SEL" lines to control register board for I/O control of the 8200.

7.12 Input

7.121 8201-D Digital Module Plug-in

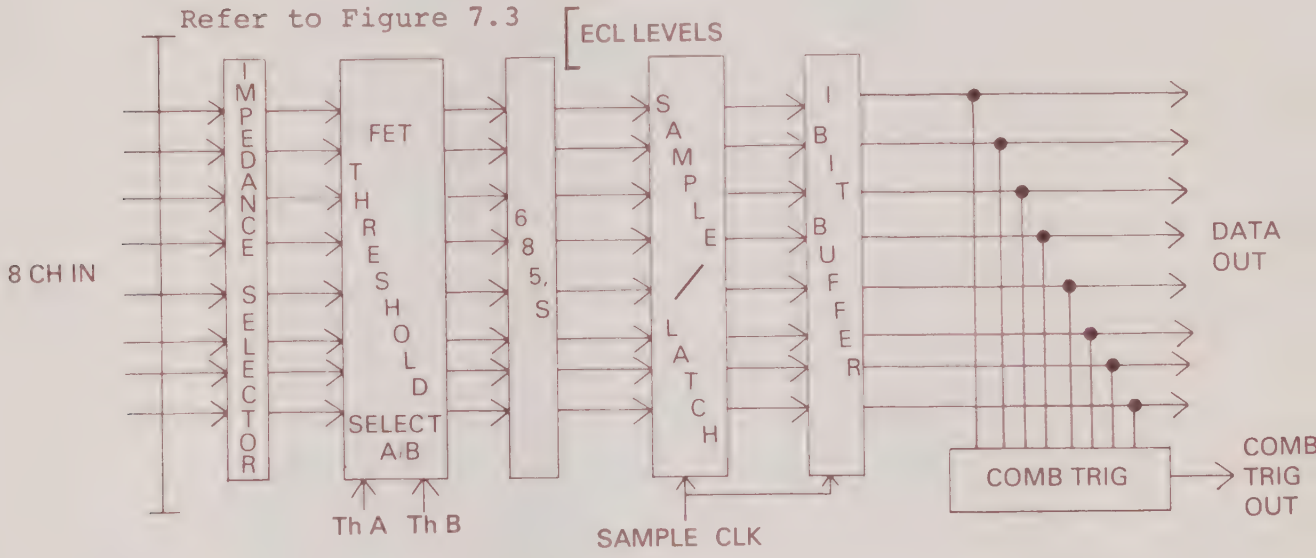


Figure 7.3 8201-D Digital Module Plug-in

1. Impedance selection is done by means of two relays, one for 50 Ω to GND and the other for 50 Ω to -2 V.

2. The FETs are used for protection of the 685 comparator. Both AC balance and DC balance are adjusted at the FET. Threshold determination is also done at the FET.

3. The 685 comparator converts the threshold determination into ECL levels.

4. In latch mode the 685 output is fed to the set/reset inputs of the first F/F. When in sample mode the noninverting output of the 685 is fed to the F/F as the "D" input to be clocked by the sample clock.

5. The state of the first F/F is then clocked into another F/F (1-bit buffer). The output of this buffer is then available as "serial data" input to the memory boards and also to the combinational trigger selection.

6. (EXMP CHAN 1). Exclusive or "U1E" determines the trigger polarity. Or gate "U1D" is either +, -, or "Don't Care." "X" input high disables the trigger decision from its data by satisfying the "or" gate.

7.13 Memory

(IN) Data is clocked into two 4-bit shift registers by eight sample clock pulses (see Figure 7.4). Byte clock then stores an 8-bit parallel word into latches. Output of latches is converted to TTL levels for memories, followed by MEM WRT to memories.

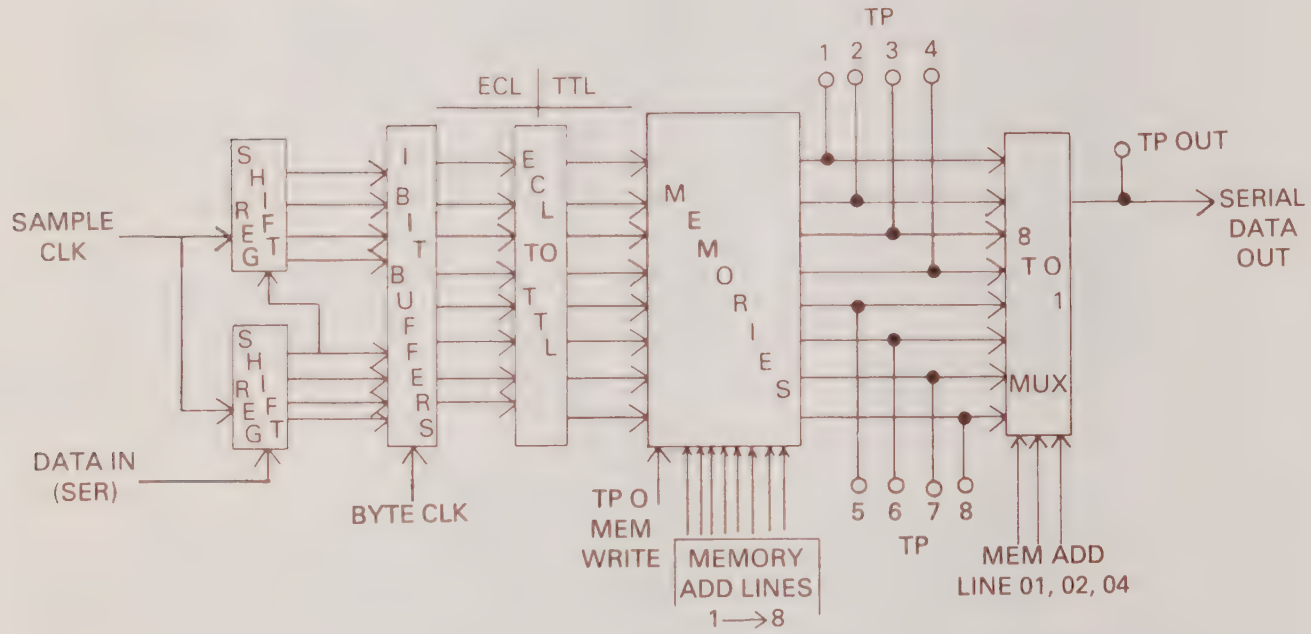


Figure 7.4

(OUT) Data is available from memories as an 8-bit parallel word. Serial conversion is done by an 8:1 mux. Address lines are synchronous to sample clock (see Figure 7.5).

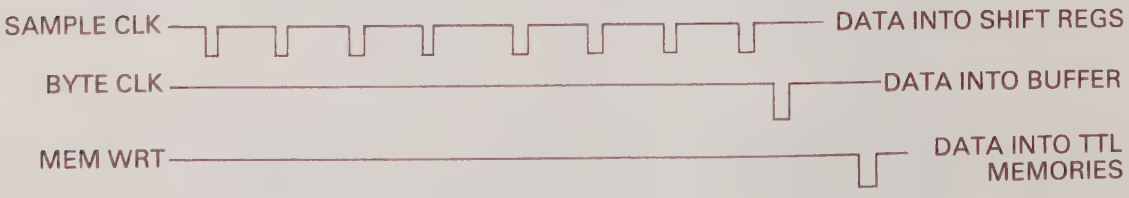


Figure 7.5

7.14 Display Board (Data Flow)

Refer to Figure 7.6.

Figure 7.6 Data Flow

1. Data from all memories are presented to an 8:1 mux (3A) on the display board. Synchronization is controlled by "DCSWPA01, 2, 4." During each memory's respective time, the complete content of the memories is transferred as a displacement on the vertical axis (data can be seen on serial data, sync swpø).

2. Data size is adjusted by a 50 K potentiometer in series with the data.

3. The waveforms for the CRT display format are constantly running when not in record. Memory data is synchronized with the display forms and is viewed as a deflection of the vertical axis.

7.15 Pretrigger and Delayed/Single or Dual

7.151 Pretrigger Single/Dual

The pretrigger single (see Figure 7.7a) start cycle (11D) is initiated by the end of the record cycle. This enables "Adr Last Mem" to set the "Ary" flop at 12E. If at this point the unit is in single mode, then the unit halts and waits for an "Arm". If the unit is not in single mode, then "Ary", which is set, passes through gate 16F and sets the "Arm" flop 15E. When the arm flop 15E is set, it resets the "Ary" flop 12E, which in turn resets the "Arm" flop 15E. "Armed" 12E is set by "Arm" FF, which stores the arm condition.

When "Arm" occurs, it passes through gate 15D to set the record latch at 15C. The first step upon entry into record is to clear both the time base counters and the memory address registers to zero. The second step is to reset Record End, and the final step of record is "Neg Rec +2" at 15B. This enables the record gate at 13D and sends the unit into record mode.

"Armed" 12E sets "Try" FF 16C, 16D and enables the "Trg" flop at 15E. The unit will remain in record until a trigger event occurs. The trigger event can come from either "Auto Mode"

or "Ext Trig" to set the "Trig" FF 15E. If there is a trigger delay set in the "Endα", FF will be set at the end of the trigger delay. If no delay is selected, then "Endα" will be set through gate 12C. When "Endα" is set, it then sets the "stop" flop 13C. Stop then enables "Store Adr 1, 2, 3". Store Adr 1 and 2 latch the most significant 8 bits of the memory address counter to record the address of the trigger event. Store Adr 3 goes to the clock generator to exit immediately from record. From this point "Rec End" is set, resetting the record latch for synchronous exit from record.

In the pretrigger dual mode (see Figure 7.7b), the trigger event 15E is used to change from main to alternate time base 13C. The selected trigger delay is still in effect as in pretrigger single. It controls the amount of words to be recorded after the trigger event.

Pretrigger dual differs from single in that the "Trg" F/F output through 14E-6 through 14E-8 clocks the "TB" Main F/F (13C) into "Alt TB" mode for the time computed by trig delay settings.

7.152 Delayed Single/Dual

Refer to Figure 7.8a. "Start Cycle" is a lockout to prevent the unit from arming and initiating another machine cycle while it is already in the midst of one. When the unit completes a record cycle, "Start Cycle" is set, allowing "Adr Last Mem" to set "Ary" 12E. "Ary" resets "Start Cycle" 11D, thereby disabling the initiation of a new sequence until exit from record. If the unit is in single mode, the machine will halt and await a manual or ext arm. If the unit is in auto or normal trig modes, then "Ary" will set "Arm." Arm will then reset Ary, causing "Arm" also to be reset. "Arm" sets "Try" and the unit goes to a trigger ready state and awaits a trigger signal.

The trigger event can come from one of three entries - auto, manual, or external. When trigger occurs, it acts as a clock to the Trg FF 15E. Trg resets the "Armed" FF and sets the record latch 15C, 15D. When the record latch is set, it clears the time base counters and the memory address registers. Record gate also resets "Endα" and resets "Stop" with the first memory "Adr Clk 2." "Neg Rec +1" 15B resets the "Rec End" flop and "Neg Rec +2" 15B sets the record gate to send the unit into record mode.

When the memory address counters count to overflow (>2048), then "Ad Madr Of1" enters the mode control board and sets the stop flop at 13C. When stop is set, "Store Adr 1, 2, 3" are enacted. "Store Adr 1" and "Store Adr 2" are used to latch the last memory address for display reference. "Store Adr 3" is used for immediate exit from record.

The stop flop 13C sets record end 14B and resets the record latch. This is preceded by resetting "Neg Rec +1" and "Neg Rec +2". The termination of the record latch sets the "Start Cycle" flop at 11D, thereby enabling "Adr Last Mem" to set the "Ary" flop 12E and restart the cycle.

When in delayed dual (see Figure 7.8b), the trigger event initiates record and the countdown for the trigger delay. At the end of the delay countdown, the Main/Alt time base latch switches to alternate time base for the remainder of the 2048 counts of memory record. As opposed to single time base mode, there is no delay to record. The selected delay controls the number of memory words to be recorded at the main time base rate.

Delayed dual differs from delayed single in that "Trig" F/F output is used to set the record latch, by passing the trig delay count through gate 15D. Upon the mode control receiving "to N END," this signal through gate 14E clocks F/F 13C (TB Main) into "Alt TB" mode for the remainder of record.

7.16 Operational Modes

The basic machine cycle is constant. The selection of modes "single, auto, normal" either accommodate or disrupt this cycle. See mode control schematic for the following descriptions.

7.161 Single

The "single" mode of operation enables the arm function as a prerequisite for trigger. When the machine exits from record mode, the machine cycle on the mode control board will halt (with the Arm Ready Led on) and will await a manual or external arm signal to advance the machine to the trigger ready state.

The "Ary" level normally passes through gate 16F to clock the "Arm" F/F. When in single mode this gate is disabled by a Low output on pin 9 of the "Single Trig" F/F 12E, thereby halting the machine cycle until receipt of a manual or external arm command through "or gate" 16C to clock the Arm F/F. The real function of single trigger mode is to inject into the machine flow the Arm function.

7.162 Normal

The normal mode of operation, in effect, bypasses or eliminates the arm function as a prerequisite to trigger. The machine, upon exiting record, will pass through the arm function by using the "Arm Ready" as an internal arm and will advance to the "Trig Ready" state awaiting an internal or external trigger.

In normal mode, the arm function is bypassed by "single trig" F/F 12E-9 being high and enabling gate 16F, thereby allowing the "Ary" level to arm the unit each cycle. With 12E-4 high, gate 12D is disabled, disabling the "trig pulser" 11D, and thereby allowing either a "manual trig" command or an external trig command from the "trig delay" board to clock the "TRG" F/F 15E.

7.163 Auto

The auto mode of operation is considered a setup mode. Logically it eliminates the need for an external or manual arm in the same design the normal mode does. Auto mode generates an internal trigger to force the machine into a record cycle, thereby also eliminating the need for an external or internal trigger.

In "auto" mode, "single trig" F/F 12E-9 is high allowing Arm ready to arm the unit as in normal mode. Auto differs from normal in that "auto-trig" F/F 12E-4 is low in "auto" mode. This enables gate 12D-6, thereby enabling the trig pulser 11D. The "trig pulser" is driven by clock pulses from the time base. With this unit enabled, the "TRG" F/F 15E receives a constant flow of clock pulses to set "trig" whenever its normal flow cycle time allows.

7.17 Trigger and Arm

7.171 Manual Arm

Manual arm on the front panel sets F/F 15E-5 on the Control Register high. This stored condition is then fed to gate 12D-1 on the mode control (both manual and Ext Arm come through "or" gate 12D). The "Arm" goes through one gate on 16E to another 16E gate where it is enabled only if 16E-10 is high (single mode). It then passes through "or" gate 16C and becomes a clock pulse to D-flop 15E. 15E-9 can only be clocked high when 15E-12 is high (15E-12 is Arm Ready). See Figure 7.9.

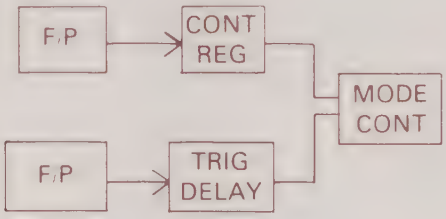


Figure 7.9 Arm

6C, and 6D. Any count greater than zero disables gate 4C and produces a logic one at 6P-11. This maintains "TD Dly End" low and through F/F 6E maintains "TD TRG DLY END" low at 6F-8. The sample clock comes through 4E-4 and 5A-8 and acts as the count down pulses for the delay counter. Once the delay counter reaches zero, 6F-11 becomes low. This clocks 5B back to its original state putting "TD Dly End" high. F/F 6E is clocked low, which breaks gate 6F allowing "TD Trig Dly End" to go high. "TD Trig Dly End" enters the mode control through 16A, 12A, and 15A and enables record gate 15C to start record.

7.18 Display

All timings for the display cycle are derived by counters 11D, 11F, 12F, 13F, and 14F. Counters 11F, 12F, and 13F have 2048 counts to overflow, providing the necessary divisions for 2048 memory positions. Each overflow pulse from 13F enables counter 11D (fly-back and blanking) to allow for Z axis or CRT blanking on CRT fly-back. The overflow from counter 11D sets "F-fly" counter allowing the sweep counters 11F, 12F, and 13F to count one horizontal sweep.

High order counter 14F is used to develop the vertical timings for display. Counts 0-7 are used to enable the seven character sweeps the character generator needs. Counts 8-15 provide the eight vertical positions for the data sweeps.

All character timings and enables are developed from counters 11F, 12F, and 13F. TBA is the enable to the character generator for Main TB, TBB is the enable to the character generator for Alt TB, TBX is the enable to the character generator for expansion, TBD is the enable to the character generator for the cursor position count. TBV is an analog voltage reference for an analog plug-in (not used on the 8200-D). See Photograph 2 on page 76.

The horizontal sweeps are derived from the Horizontal DAC. The timings for the DAC are provided from 11F, 12F, and 13F. Each full count from 11F, 12F, and 13F provide the count pulse to 14F. This enables 16 full sweeps of the counters and 16 sweeps from the horizontal.

The vertical DAC is driven by SWP ADDs 1, 2, 3, and 4 for the vertical displacement. SWP ADD 4 is used to define character time sweeps (smaller increments) from data time.

The Z axis is driven by either serial characters from the character generator or memory data from the individual memories. All timings for characters and data are derived from counters 11F, 12F, 13F, and 14F.

All further writings will refer to Photos 1 through 5 on the following page for explanations of the display cycle.

1. SWP Ø is the first position in the high order counter (see Photo 1). It represents the beginning of the display cycle and is available at TP SWP Ø. (Note that all signals shown are available as test point.)

2. The HORIZ on Photo 1 provides 16 sweeps per display cycle for the seven character sweeps and eight data sweeps.

3. The VERT DAC output shows the seven character sweeps as slight level changes, while the eight data positions reflect a greater difference between steps. The character generator requires seven sweeps to trace a character while each data channel requires only one sweep (see Photo 2).

4. Sweep AD 1, 2, 3, 4 (the output of counter 14F) provides the timing scheme for the display. Sweep times 1-7 provide the timings for the seven sweeps. A comparison of SWP AD 1, Z, and CHAR reflect this timing.

5. Within each character sweep, as shown in Photo 3, blanking occurs previous to each data sweep and each character sweep. There are four enable times (TBA, TBB, TBX, and TBD). These enables are presented to the "char gen" board for data enables. Photo 4 shows the relationship of DOT SEL 1, 2, and 4 to each data enable. DOT SEL 1, 2, and 4 are timing signals to the "char gen" board to read out the characters in serial for the Z axis.

6. Sweep times 8-15 (SWP AD 4 high) are allotted to data display. The "data" input on Photo 5 enables the "Z" axis for the data sweeps. Each count of SWP AD 1 consists of 2048 sub-counts for reading out memory data onto the display. Within "SWP AD 4" positive time there are eight counts of "SWP AD 1", one count for each memory. Serial Dig is fed into the VERT DAC as an offset at the output. (Serial Dig is memory data.)

7. The cursors are also fed onto the VERT DAC as an offset in its respective time. The timing of the cursors (its sweep position) is determined on the "cursor control" board and enabled onto the VERT DAC at "SWP AD 4" positive time.

7.19 Record

Refer to Figure 7.12. When Mode Control Record is set, STOR ADD 3 is clocked low. This signal passes through 6A and is synchronized with ADD CLK 2 at 3C-15. The level enables gate 4C with "Record". The level is then synchronized with the byte clock at 3C-3. 3C-3 enables gate 5D. The "Record" level is used to derive a one shot at 4C-3 to reset the sample byte clock counter at 7C.

When gate 5D is enabled, that is, input pin 5 no longer holds the gate satisfied, then input pin 4 is allowed to control the gate. Gate 9C is set by byte counter 7C. It is reset through gate 5D-4. The memory write clock is synchronized to the byte clock by its origin, the byte count counter. This set-reset function continues for as long as the machine is in record and acts as the memory write pulse generator. The byte clock and the memory write clock are derived as a specific count of the byte clock counter.

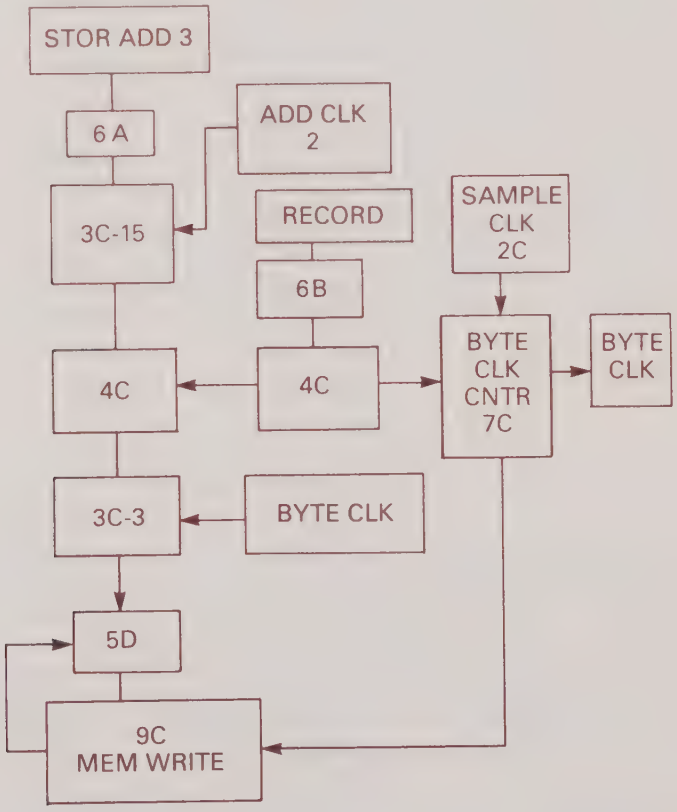


Figure 7.12 Clock Generator

7.20 Remote Input/Output

7.201 Overview

The remote I/O board acts as a system controller for data transfers to and from the 8200. Both front panel external program switches must be engaged simultaneously for entry into "EXT PRG" mode.

See Figure 7.13. The "Command" along with the command data are interpreted and transferred to the trigger delay board and the control register by means of the "RI BUF SEL" lines as a function select and the "RI DAT 1-8" lines as options within a given function. The "RI $\overline{\text{TCMD}}$" is the enable signal to the trigger delay and "RI NCPCR" is the enable signal to the control register. All control register outputs are available to the remote I/O board. The Read/Write bit (OC-5) determines whether these outputs are transferred as data out or ignored as in a write command mode.

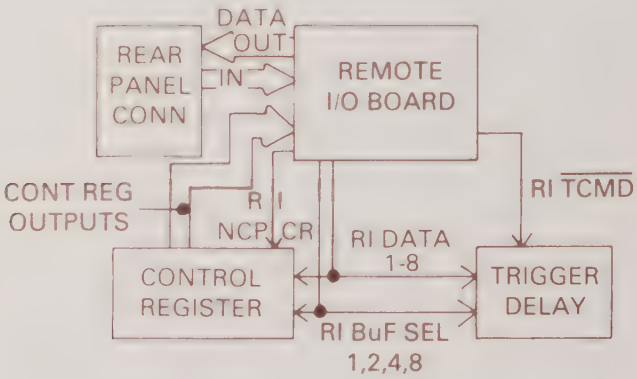


Figure 7.13

7.202 Command - Flag

The remote I/O system has the basic requirement that all data to be written into the 8200 must be present previous to the "Command" that acts as an enable.

See Figure 7.14. The "Command" pulse received by the 8200 is used to implement the "Flag" out of the 8200. The "Flag" is used also to generate the output enable. The data-out is valid only when Flag is enabled.

The "Command-Flag" relationship acts independent of the data in and out. When a command is received and the address and polarity requirements are satisfied, then it is a timed sequence from "Command" to "Flag". The time is fixed by design. There are commands that will be in process when flag is returned. The external operator must keep track of these.

"RI NCPCR" is generated off of the "RI TCMD" and is used to enable the external command information to the control register board.

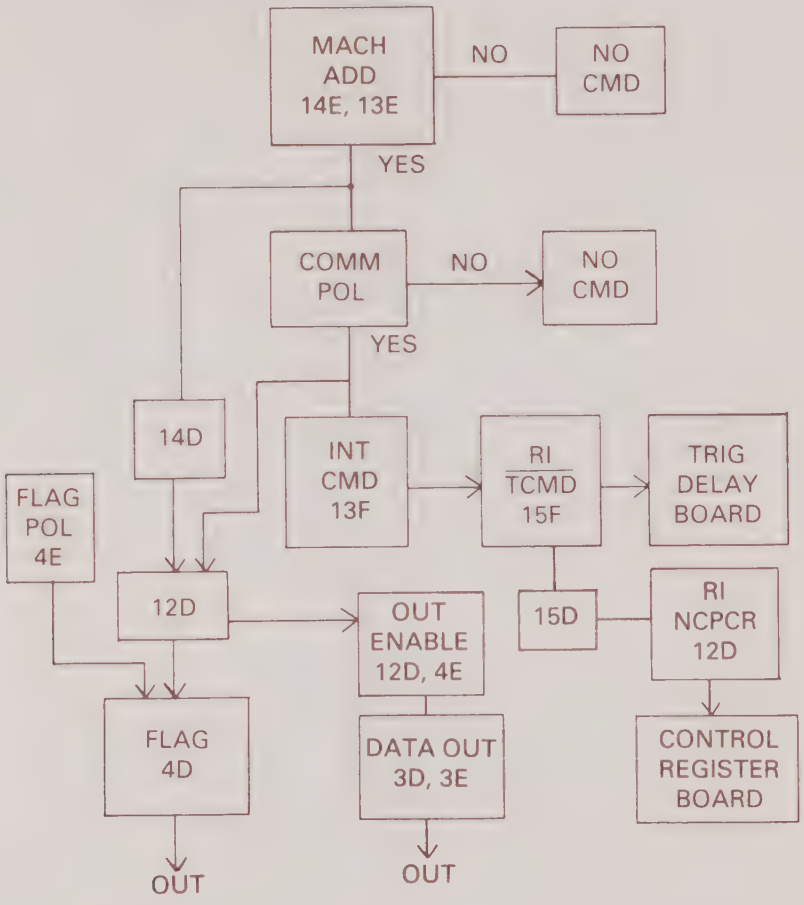


Figure 7.14

7.203 Data In

All references are to the remote I/O board except when noted.

OC-5 of the data word is the Read/Write bit. Write is enabled when OC-5 is high.

OC-1, OC-2, OC-3, and OC-4 are the internal function select bits.

DO-1 through DO-8 provide the internal selection of options within a given function.

See Figure 7.15. The function select and data bits are fed directly to the control register board to a 2:1 Mux 74157. "RIO EXT PRG" is required to select the "RI BUF SEL" at the mux and "RI NCPCR" enables the 74157's, thereby writing the desired information into the control registers.

When OC-5 is high, it enables "TCMD" through gate 15D to become "RI NCPCR," the 74157 mux enable pulse.

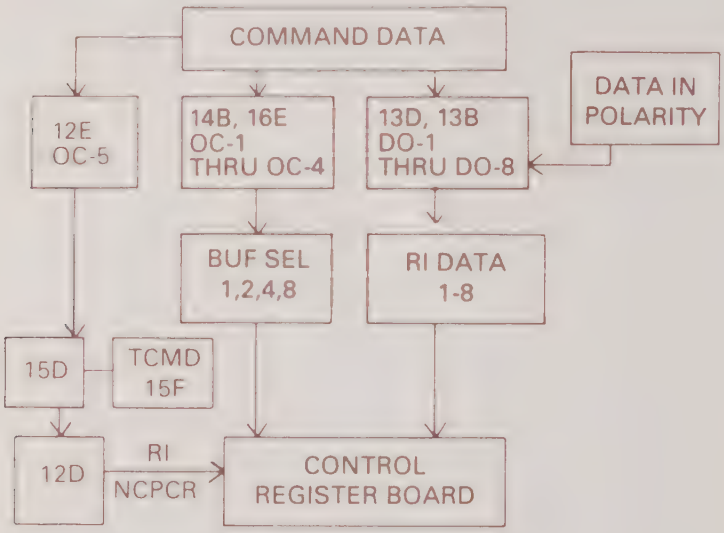


Figure 7.15

7.204 Data Out

To enable valid data out from the 8200, a read command must be initiated. OC-5 being low is the requirement for a read command.

The difference between a read and a write command is that OC-5 being low disables the gating of "TCMD" to become "RI NCPCR" at gate 15D. Read command disables the command input enable to the control register.

See Figure 7.16. All control register board outputs are available to a series of 8:1 mux (74151's) on the remote I/O board. The read commands function select bits are used as address bits to the 74151's. Because there are two banks of 8:1 mux's, OC-4 becomes the bank selection bit. These bits may be viewed at TPAØ through A3, AØ being the lowest order.

The outputs of both banks pass through "or gates" 2E and 2F, to convert both banks to one data bus. Gates 2D and 3F are used for data out polarity and gates 3D and 3E are the output enable "and" gates.

In addition to identifying the source and destination boards in the signal name, a negative level active signal is identified by an N following the source board abbreviated name. For example, DC N Swp Ad 4 is a signal originating on the Display Control Board and the signal is Negative Sweep Address 4. Names without N following the source initials are positive active. The original intent with regard to logic notation was that all negative active signals emanate from logic gate and device symbols with balloon outputs, such as positive input negative output nand gates. The convention used on clock pulses was that the trailing edge be the active edge, such that the positive going edge of negative clock pulses cause clocking action in flip-flops and counters. For devices using the negative going edge, the clock pulse is positive to maintain synchronized clocking operation throughout the instrument. Exceptions to this convention will be explained in the text for that circuit.

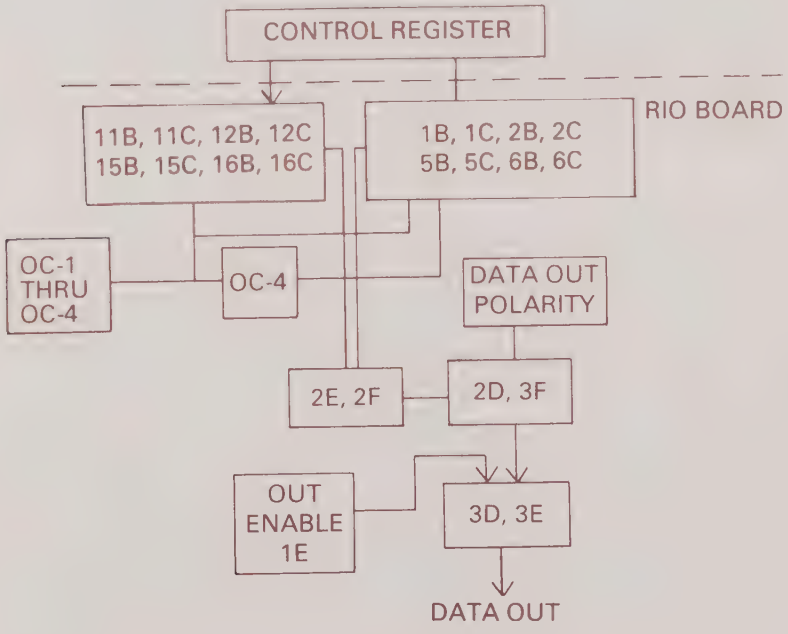


Figure 7.16

7.2 Circuit Analysis

7.21 Input Circuit (Digital Module Logic Board)

The data input circuits are on the Plug-In Logic PC Board and the Arm and Trigger external input circuits, which are identical to the data input circuits, are located on the Trigger Delay PC Board. Because all ten input circuits are identical, only Channel 1 Data Input Circuit will be described. Referring to the upper left corner of the schematic, the double DIP relay K9E is used to select the input termination. The controls are shown in the relaxed position for both relays. R56E and R55E form a split termination for the 50-Ω coax cable from the front panel. All eight coax cables for the data channels are of equal length to minimize circuit delay differences between channels from the front panel to the first rank of flip-flops where common clock pulse timing resynchronizes the channel-to-channel data timing. When the lower relay in K9E is activated, R56E becomes connected to -5.2V and R55E becomes connected to ground. The parallel combination of R56E and R55E are approximately 50Ω, and the Thevinin equivalent voltage at the end of the coax is approximately -2 V. This termination is then an effective load for a typical ECL logic circuit operated from ground and -5.2 V as Vcc and Vee respectively.

This split termination technique is used extensively in the 8200 and will be referred to for simplicity as a "termination to -2 V." When the upper relay is operated, and the lower relay is left deenergized in K9E, both resistors R56E and R55E are connected to ground. Again, the parallel resistance of the pair is 50Ω, and the termination is to ground. When both relays in K9E are left deenergized, the resistors are not connected. Also, the effective input impedance is R58E to 15 V in parrallel with the series combination of R52E and R54E to -15 V, all shunted by the input cable capacitance, or approximately 1 MΩ to ground shunted by 30 pF to ground. The trimmer C33E is used to achieve AC balance in the input biasing network in the same fashion as the AC trimmer is used in most passive oscilloscope probes.

As can be seen, this input network is used to drive the gate of one-half of the matched FET follower pair, Q8E. The biasing network has a gain factor of 10/11. The other FET follower of the pair has its gate driven through a similar network by a selectable DC threshold voltage. However, the input network on the threshold side does not have a trimmer capacitor, but instead has a trimmer resistor R45E. The trimmer resistor is placed in the network so as to provide an input offset voltage adjustment to correct for all component tolerance and FET V_{GS} offset voltage and offset voltage in the comparator U8E. The source terminals of the FETs at Q8E are back-to-back diode clamped by CR5E and CR6E, and R53E and R49E are the source current bias resistors. With this circuit, the input from the front panel may be driven to plus or minus 50 V without damage to the circuit, except for the possible exceeding of the power dissipation limits of R56E and R55E if the input termination is selected to be 50Ω.

The high-speed voltage comparator U8E, is a differential analog/input device with complementary digital ECL open emitter outputs. It is capable of detecting input changes of several millivolts and switching output state with propagation delays in the 5 to 10 nsec range, depending on the input voltage overdrive. The true output of the comparator is used to drive the "D" input of the edge triggered flip-flop U6E, and at this point the data is synchronized to the clock system. When the data inputs are being operated in the "Sample Mode," the "R" and "S" inputs to the flip-flop U6E are held low and inactive, and the "D" and clock pulse inputs control the action of the flip-flop. As stated before, the outputs of the voltage comparator are ECL, with voltage swings typically from -1.0 V (positive level) to -2.0 V (negative level).

For convention, as with flip-flops, the upper output is the true output and the lower output, with the balloon or bubble, is the complementary output. All ECL output and input terminals are further identified by the half arrowhead at those terminals, pointed in for inputs and pointed out for outputs. When the data inputs are operated in the "Latch Mode,"

one input in each of the two gates in U7E, pins 5 and 12, are driven low by the signal N Latch Enable. Consider a set of circumstances in which both flip-flops in U6E have been set. Pins 3 and 14 of U6E are low because of previous data input conditions, and now a narrow snig of negative polarity occurs on the data input, sufficient in magnitude to cause the comparator to produce opposite polarity snigs on its outputs. Pin 7 produces a negative snig that also appears on pin 10 of the gate at U7E. This fulfills all the "and" requirements of the gate, and the gate output and pin 14 produce a positive snig that resets the flip-flop at U6E asynchronously through pin 4.

The "D" input to the flip-flop, pin 7, also sees the negative snig, and if the effective edge of the clock pulse occurs within the time of the snig or the "D" input, the snig on the "R" input, pin 4, overrides. If the effective edge of the clock pulse does not occur during the time of the snig, then the next effective clock pulse edge following the snig will cause the flip-flop to be set because the "D" input to the flip-flop is high at that time.

Tha action of the second flip-flop in the string, with outputs on U6E pins 15 and 14, is to accept sychronously data from the first flip-flop, ensuring each data bit to be a full data point wide, and present it to the channel memory for storage. Its outputs are also fed back to the inputs of the steering gates to enable complement data being entered in the first rank flip-flop. In this fashion, each detected snig is stretched to one full data point wide for storage, and synchronized with the data in the other channels to prevent channel-to-channel time skew in the data. The output of each channel second rank flip-flop is taken directly via coax cables to its respective Channel Memory PC Board.

In addition, the complement outputs of each of the channels second rank flip-flops are used as inputs to the combinational triggering circuits. This logic might be more easily understood when considered from the output backward toward the inputs. The two negative input negative output and gates at U2C are emitter "or" tied with the preload termination being at the destination end of the coax cable into which they are fed. If the criteria for either gate is not met for its output to be low, that output pulls the other gate high. This creates logically an eight negative input, single negative output and gate, and the output signal is DP N In. Comb., or Digital Plug-In Negative Internal Combination (Trigger). The input criteria to the gate is then negative for each channel to cause trigger. If the X_1 input (don't care) to the nor gate V1D pin 7 is held high, channel one criteria for trigger is met regardless of the condition of V1D pin 6. Each channel combinational-trigger three-position selection switch on the plug-in front panel provides a high-level signal on its X line if, and only if, the switch is in

the centered position, which is the X (don't care) position. In addition, a low-level signal is provided on the 0 line from the switch. If the switch is up, in the 1 position, both the X and O lines have low-level signals on them. If the switch is down, in the O position, the X line has a low-level signal on it and the O line has a high-level signal on it.

Referring back to pin 6 of the nor gate V1D, the criteria for this input is to be high if, and only if, the selected 1 or 0 switch position is met by the flip-flop. The exclusive nor gate at U1E, output pin 2, is used in this application as a controlled polarity buffer. If the input pin 5 is held high, the output pin 2 follows the other input, pin 3. If the input pin 5 is held low, the output pin 2 is the complement of the input pin 3.

The clock pulse circuitry on this board is part of the clock pulse distribution system and will be covered in that paragraph.

The split terminations to -2 V, as mentioned previously, are required to terminate each ECL circuit that has a destination circuit connected to it. In those cases where the signal path exceeds one inch in length, more or less, the signal is routed through a 50Ω coax cable. In this case, the termination is 50Ω and is always at the load end of the line. In most cases where a coax cable is used, and in every case in which a signal leaves one board in the instrument and is routed to another board via coax, a dedicated driver and a dedicated receiver are used, providing no fan-out directly from the cable. In some cases where the signal repetition rate is lower that 200 MHz, i.e., it is not routed through coax cable, and where the speed requirement to maintain synchronization is relaxed, split terminations of 100Ω and 200Ω have been used to ease the current requirements on the -5.2 V power supply.

7.22 Data Storage

Each data channel output coax cable from the data input circuits is an equal length cable to the input of the appropriate Channel Memory PC Board. There are eight identical interchangeable Channel Memory PC Boards or Channel Memories, and the channel designation is made by location on the Memory Mother Board into which the Channel Memories are plugged. This Memory Mother Board is directly behind the Plug-In Logic Board, and has mounted on it the coax connectors and multi-pin connectors through which power supply voltage, control signals, and high speed signals are communicated between the main frame and the plug-in module.

The data input to the Channel Memory is terminated on that board, and is input directly to the serial input of the

first of two serially connected 4-bit shift registers, U10 and U18 respectively. These shift registers are "serial-in/ parallel-out" ECL devices, the inputs being first-stage edge-triggered D inputs, triggered by the positive going edge of the clock pulse, and data is advanced in the register by the same clock pulse action. The Clock pulse operating this shift register is the same frequency and timing as the clock pulse operating the flip-flops in the data input circuits in the plug-in module. The parallel outputs of the shift register are fed directly into the D inputs of eight flip-flops at U5, U9, U17, and U22. After 8 bits of data are advanced into the shift register, a "byte" clock pulse transfers that data into the eight flip-flops, which are a holding register for the data inputs to the memory circuits U1, U2, U6, U7, U15, U16, U19, and U20. The data flow to this point has been ECL level, and the memory chips are SN74S200 type 256 address by 1-bit Schottky TTL memories, so each of the holding register flip-flop outputs is fed through an ECL to TTL level converter circuit. There are two circuits at U8 and U21 to serve this function.

There is one additional set of circuits on each Channel Memory that are important in maintaining strict timing relationships between signals during the data recording process. There are two chips, U12 and U13, each of which is a 4-bit "parallel-in/parallel-out" edge-triggered D flip-flop register. These flip-flops contain the memory address for recording and for retrieval. The eight inputs are generated on the Address Control PC Board. The clock pulse is generated on the Clock Generator PC Board, and its timing is such that its effective edge occurs after the trailing edge of the Memory Write Enable pulse to staisfy the "hold" requirements of the memory circuits during recording, regardless of the selected record rate, or sample interval. Timing for this clock pulse, and for the Memory Write Enable is achieved on the Clock Generator PC Board, and will be discussed in that section.

A noninverting ECL gate chip at U14 provides fan-out buffering for the Sample Interval Clock Pulse for the input shift register and for the Byte Clock Pulse for the holding register. A Schottky TTL hex-inverter chip at U3 provides fan-out buffering for the address register clock pulse, the Memory Write Enable pulse, and for the address register "power-on" reset pulse. One additional buffer in U3 is used for the Memory Write Enable test point (MWT).

One additional circuit on the Channel Memory is the eight-input data multiplexer at U11. This circuit, used only for retrieval, serves to reverse the process achieved during storage by the input shift register and holding register. For a single memory address, common to all memory circuits, this multiplexer selects one bit at a time each of the memory

circuit outputs and creates a serial bit stream of the 8 bits, in the same sequence as when they entered the shift register during recording. The three control lines used for controlling this multiplexing are generated on the Address Control PC Board and will be discussed in that section.

7.23 Time Base

Time Base and Clock Pulse Generation and Synchronization

The portion of operation of the 8200 requiring the greatest care in clock pulse timing and synchronization is the recording of data at the fastest clock pulse rate (or Sample Interval of 5 nsec) or nanoseconds. At this Sample Interval, or Time Base, the record clock pulse, or Sample Interval clock pulse, occurs at intervals of 5 nsec and is nominally a square wave. The Byte clock pulse is synchronous with the "last of 8" Sample Interval clock pulses. The generation and distribution of these clock pulses, as well as the Memory Write Enable pulse, the Memory Address clock pulse, Sample Interval clock pulses for the plug-in module, the Trigger Delay circuits, and for external use are all accomplished on the Clock Generator PC Board.

Referring to the Clock Generator schematic diagram, in the upper left-hand corner, the basic frequency source is a 200 MHz ECL output crystal oscillator. This frequency is used directly, except for buffering, for the fastest record rate, or shortest Sample Interval, of 5 nsec. All other frequencies are counted down from this in 1, 2, 5 sequence for the longer Sample Interval clock pulses. The four fastest rate clock pulses, 5 nsec, 10 nsec, 20 nsec, and 50 nsec are generated and distributed directly on the Clock Generator PC Board. For all lower frequencies, the 50-nsec clock pulse is converted to TTL level, sent to the Time Base PC Board, and counted down in TTL circuits to the lowest record rate, or 5-sec Sample Interval. The selected Sample Interval clock pulse is then returned to the Clock Generator PC Board, converted from TTL to ECL level, and distributed to the parts of the instrument involved with recording and record rate synchronization.

The flip-flop at 1D is used to divide the 200 MHz to 100 MHz. Its output, pin 2, is used to clock a divide by 2 and divide by 5 counter at 1E to obtain 50-MHz and 20-MHz clock pulses respectively. Each of these four frequencies is used as an input to each of the steering gates at 3D, 200 MHz to 3D04, 100 MHz to 3D06, 50 MHz to 3D11, and 20 MHz to 3D13. The frequency selection control lines are obtained from the Time Base PC Board and are such that when one of the four fastest rates are selected, it is low level and the other three are high level. However, when none of the four are selected, all four are low. Therefore, the four input TTL nor gates at 7A, the four exclusive or gates at 8B, and the TTL to ECL converters at 7B are used to provide the correct

controls for the gates at 3B. Also, one of the inputs to the four input or gates at 4D will have the selected clock signal on it, or all will be low level if one of the lower frequencies has been selected. In that case, pin 6 of the nor gate at 1C will be low level, and the selected frequency will be on pin 7 of that nor gate after being selected on the Time Base PC Board and sent as either TB Main or TB Alt, converted to ECL level and gated together at or gate 2B pins 13 and 12.

The lower left corner of the schematic illustrates the circuits used to select, terminate, and input the External Time Base from the front panel of the instrument, making it possible to synchronize the sampling and storing of the data at the inputs to the instrument with the clock pulse that generated the data. The output of the gate at B1 pin 11 is high when External Time Base is selected. When the termination selection at B109 is high (selecting ECL ternination), the output pin 8 in low, driving the coil of relay K1, closing its contacts, and forming a signal path for the External Time Base input ot the split termination R25 and R26 as well as to buffer gate input pin 2B04. If the termination selected is TTL, the gate output 1B03 is high and gate output 1B06 is low, driving the coil of relay K2, closing its contacts, and forming a signal path for the External Time Base input to the termination R27 and the input pin 5 of the TTL to ECL converter at 3A. The nor gate inputs pins 4 and 5 of 3B accept the chosen signal, and pin 2 in turn drives the input pin 11 of the gate at 1C.

The complementary output pins of the TTL to ECL converter at 3A drive the two control inputs, pins 10 and 5 of the gates at 1C, selecting the correct one of the two gates and selecting the Internal or External Time Base to appear at the nor gate output pin 1C15. At this point all sources of clock pulses for storing data become common, and from this point all propagation delays in clock pulse circuits for data recording are strictly accounted for and adjusted where necessary for component tolerance. This is an absolute necessity with circuits that nominally exhibit propagation delays for a single gate approximately equal to one-fourth of one 5-nsec Sample Interval, which is also approximately equal to the propagation delay in 10 in. of properly terminated coaxial cable.

The Time Base signal at this point drives three buffer gates at 2C. The gate output at pin 2 drives two more buffer gates, one of which drives the Time Base clock pulse to the plug-in module, and the other drives the Time Base clock pulse to the Trigger Delay PC Board for the Arm and Trigger sychronizing circuits. The gate output pin 2C14 drives a dedicated coax cable directly to a divide by 10 counter on the Trigger Delay PC Board. The gate output pin at 2C03, with additional buffering, drives the Sample Interval clock pulse

circuits for recording, the Byte Clock Pulse timing circuits and Byte Clock Pulse buffers, Memory Write Enable timing circuits, and Memory Address Clock Pulse timing and drive circuits.

The gate output pin 2C03, through gate 9C03 and gate 9C02, and the two parallel gates at 10B02 and 10B15 drive the eight parallel gates in the circuits at 10A and 11A. Each of these eight gate outputs drives through a coax cable of equal length to each of the other seven cables and equal length to each of the eight Byte Clock Pulse cables to one of the Channel Memory PC Boards. The number of circuit delays for the Byte Clock Pulse signals is the same, starting at gate output 2C03, again through the gate at 9C03, the gate at 6C14, the two parallel gates at 9B03 and 9B14 that drive the eight parallel gates at 8A and 9A. The gate output at 2C03 also drives the clock pulse input of the 4-bit binary counter at 7C.

The least significant 3 bits of this counter provide the eight counts enabling the gates at 9B to decode the 8th count for the Byte Clock Pulse, and enabling the gates at 8C to decode the counts 1 and 5 for setting and resetting the RS flip-flop formed of the cross coupled gates at 9C15 and 9C14. An additional gate at 5D02 allows the insertion of another reset control to hold the flip-flop off at times other than record time. The output of the gate at 9C14 drives the ECL to TTL converter input 5A03 providing the Memory Write Enable pulse to the eight Channel Memory PC Boards. The gate output 9C14 also drives in series the two gates at 10B14 and 10B03, each of which has on its output a single preload resistor and a trimmer capacitor that allows for time adjustment of both edges of the pulse for up to 10 nsec. Another or gate at 5C allows this pulse, which is now the Record Memory Address clock pulse, to be gated with the Read Memory Address clock pulse. These two signals are controlled to be mutually exclusive, so the gate output at 5C14 and the two ECL to TTL converters at 5A13 and 5A12 have the correct clock pulse for recording, desplaying, plotting, or outputting data through the digital interface.

The two delay networks of the two resistors and two trimmer capacitors at gate outputs 10B14 and 10B03 are used to allow the use of memory chips made by different manufacturers on the Channel Memory PC Boards. Several manufacturers provide the chip, basically a SN74S200N chip, and there are some variations in the specified "set-up" and "hold" time requirements. The adjustments provide the capability to accommodate any of the approved memory devices, provided that only one manufacturer's device is used in any single 8200. No single adjustment can be made to provide correct timing of the memory address and write enable pulses to meet the requirments of mixing memory devices.

The other circuits on the Clock Generator PC Board are the 20-MHz Positive Clock Pulse, output from the ECL to TTL converter at 5A05 to drive the further clock pulse count down chain on the Time Base PC Board. A TTL to ECL converter circuit at 3A01 provides a memory address clock pulse with additional circuit delays that is used in the flip-flop at 3C11 to synchronize the end of recording. The negative byte clock pulse at 9B02 is used in the flip-flop at 3C06 to synchronize the beginning of recording, which is applied at the D input to that flip-flop after passing through the circuit delays of the TTL to ECL converter at 3A14, and the gate delays at 6B03, 6B14, 6B15, 4C14, and 4C02.

The beginning of the record control signal is also edge detected by the use of the gate delays at 6B03, 6B14, and 6B15 being applied to the gate input at 4C06, with the negative record signal from 3A13 being applied at 4C07 to provide a nominally 3-nsec wide pulse at 4C03 for use in resetting the binary counter at 7C to zero at the beginning of recording. Another gate 4C, inputs 12 and 13, creates the same pulse using the same inputs, but its output at pin 15 is used to reset the flip-flop reset pin 1D05 and the divide by 2 and divide by 5 counters reset pin 1E09. Thus all count states start at zero at the beginning of recording.

Tow additional buffer gates at 4A02 and 4A03 provide free-running Sample Interval Clock Pulses, responding only to the control of Main Time Base/Alternate Time Base, when in Dual Time Base Mode. In Single Time Base Mode, the Main Time Base is output continuously, making it possible to operate two 8200 instruments in parallel by selecting the desired Time Base, or Time Bases, on one instrument, and selecting the External Time Base, and ECL termination on both instruments, making both instruments slave to the one time base control. Two equal length 50-Ω cables may then be used to connect the External Time Base inputs of each instrument to one of the two rear panel connectors "TB Out" on the one instrument being used to provide the time base. Thus, the number of parallel data channels available is 16. Care must be exercised in the manner of providing Trigger and Arm signals, to cause the data recording to start and stop simultaneously in the instruments.

The Clock Generator PC Board is physically located in the center of the memory assembly, with four Channel Memory PC Boards mounted above it and with four mounted below it. This makes possible the use of shorter equal length coax cables for the distribution of clock pulses and data.

Time Base Counting and Control

The free-running 20-MHz Positive Clock Pulse received on the Time Base PC Board from the Clock Generator PC Board is used directly without buffering because the counter strings

using that signal are made up of negative edge-triggered decade counter circuits. Referring to the schematic diagram for the Time Base PC Board, the signal in the upper left corner of the diagram may be seen to be driving pin 14 of the circuit at 7A and also driving pin 14 of the circuit at 16A. The circuit at 7A is divide by 2 counter and a divide by 5 ripple-down counter, which in turn drives a similarly connected circuit at 7B. The four circuits 7A, 7B, 7C, and 7D are so connected, without reset capability, to provide a continuous 2-kHz clock pulse, which is buffered by the gate at 14B11, and then sent to the Remote Input/Output PC Board to be counted down to 1 kHz for use in driving the Front Panel Multiplex addressing circuits and for clocking the multiplexed front panel data into the appropriate flip-flops in the Control Register.

The circuits at 16A, 16B, 16C, 16D, 16E, 16F, 15F, and 14F are similarly connected to form an eight-decade ripple-down counted from which each of the selectable Time Base decades is derived. The counter is reset at the beginning of recording by the buffered reset pulse MC TB Counter Reset to reduce the timing relationship uncertainty between the selected time base and the effective Trigger pulse. The 2-MHz output of the circuit at 16A is buffered and sent to the display oriented PC boards for use during the Display Mode. This clock frequency is used for the data display rate, and the timing and geometry of the display will be discussed in the section covering the Display Mode.

To explain the Time Base selection gating, it is first necessary to review the nature and coding of the signals obtained from the front panel Time Base selection switches. For example, there is the Main Time Base selection switch of two single pole wafers with binary coded contacts having no direct correlation to the Time Base selected. The left lever and its wafer has nine positions ranging in 1, 2, 5 sequence from 0.1 to 50. The right wafer has four positions, nsec, usec, msec, and sec. The left wafer has four binary coded contacts, and the right wafer has two binary contacts. The codes produced from those contacts for the various positions selected is shown below.

Left Wafer Position	Contact Output	Right Wafer Position	Contact Output
0.1	0000	nsec	00
0.2	0001	µsec	01
0.5	0010	msec	10
1.0	0011	sec	11
2.0	0100		
5.0	0101		
10	0110		
20	0111		
50	1000		

These contact signals are duplicated by the Alternate Time Base selection switches and are time multiplexed with the other front panel control switch contact signals. These signals are then sent to the Control Register to be demultiplexed and stored in flip-flops, which then directly control the various circuits in the instrument requiring that control.

To consider again the Main Time Base selection, there are six flip-flops in the Control Register that represent exactly the six contact output signals from the Main Time Base selection switches, and these six flip-flop outputs are sent to the Time Base PC Board. Four of these, representing the decade wafer contacts, are called CR TB Main Decade 1, CR TB Main Decade 2, CR TB Main Decade 4, and CR TB Main Decade 8. Two more, representing the seconds wafer contacts, are called CR TB Main Seconds 1 and CR TB Main Seconds 2. The four signals representing the decade wafer are used as inputs to a four-line binary to ten-line encoder circuit at 11C. For each of the decade wafer positions to be selected, there is a single output from the circuit. These signals are further encoded by class in the gates at 12B and 12C. The six classes are tenths (0.1, 0.2, and 0.5), units (1, 2, and 5), tens (10, 20, and 50), ones (0.1, 1, and 10), twos (0.2, 2, and 20), and fives (0.5, 5, and 50).

The reason for this encoding may be made more clear by considering the output Time Base selecting circuits and multiplexers, and writing equations for the multiplexer addresses. The control input signals at pins 1, 5, and 11 of the and/or gate at 15A have the significance of ones, twos, and fives respectively. The output pin 5 of the 8:1 multiplexer at 15C will have on it the output signal of one of the decade counters in the string 16A through 14F. The multiplexer address lines at pins 11, 10, and 9 are also connected to the same exact pins of the multiplexer circuit at 15D. For any input pin on 15C, the signal is one decade longer than the signal on the same pin of 15D. For example, the signal on pin 4 of 15D is 50-nsec time base, and the signal on pin 4 of 15C is 0.5 μsec. The inverted output, pin 6, of 15D is used to count down by 2 or 4 through the two flip-flops at 15E, whose outputs are now selectable in the gates at 15A. For any given code on the three signals AMX1, AMX2, and AMX4, for example 200 (selecting pin 4 on both circuits at 15D and 15C) the three signals at the gate inputs at 15A are 1, 2, 5 sequence, and using the example, 0.1 μsec on pin 15A02, 0.2 μsec on pins 15A03, 04, and 0.5 μsec on 15A10. To write the equation for the signal AMX1:

AMX1 = (5 μsec + 2 μsec + 1 μsec) + (0.5 msec + 0.2 msec + 0.1 msec) + (50 msec + 20 msec + 10 msec) + (5 sec + 2 sec + 1 sec)

To factor AMX1 = (5 + 2 + 1) μsec + (0.5 + 0.2 + 0.1) msec +

(50 + 20 + 10) msec + (5 + 2 + 1) sec.

To paraphrase AMX1 = (units) μsec + [(tenths) + (tens)] msec

+ (units) sec.

To 13C08 = (13A09) (13A10) + [(12A04) + (12A05)] 13B12 + (13B04)

13B05.

AMX1 is the least significant of the three binary address control lines to the multiplexer circuits at 15D and 15C, with AMX2 and AMX4 being more significant in that order. Pin 7 on both circuits is the negative circuit enable input and is driven by the negative and negative out gate at 12A whose inputs are active for TB Main (not Alternate) and for other than nanosecond time base from circuits 11A08 and 11B11 respectively.

This entire coding and selection process is duplicated for the selection of the Alternate Time Base, as indicated by those circuits at the bottom of the schematic diagram, namely those circuits at 11E, 11F, 12D, 12E, 12F, 13D, 13E, 13F, 14C, 14D, 14E, and 15B, all using the same decade time base count down circuits at 16A through 14F.

7.24 Front Panel Control System

Front Panel Signal Multiplex System

All front panel switch contact signals are time division multiplexed to reduce the magnitude of wiring required in assembly of the 8200. In addition, the use of flip-flop storage registers for holding the front panel control data provides for changing the controls by means of an external control source through the proper use of the interface on the Remote Input/Output PC Board. The front panel switch contacts are, for the purpose of multiplexing, arranged in groups of eight contacts, each group being one word.

Referring to the schematic diagram for the main frame Front Panel PC Board, there are four signals introduced through the front panel PC edge connector, RI0PMAD1, RI0PMAD2, RI0PMAD4, and RI0PMADN8. These are abbreviated names for signals generated on the Remote Input/Output PC Board, called Panel Mux Address 1, 2, 4 and 8. With four address bits being derived from a binary counter, there are 16 states, or counts, of these four bits. The least significant three bits drive the address inputs of the 8:1 multiplexer, or mux, circuits at U1 through U7, except for U5, which is driven by all four. For instance, when all address bits are low, the signal on the input pin 4 of each of the mux circuits will appear on the inverted output pin 6 of each circuit. Also, the four-line binary to ten-line converter at U5 will have its selected output pin 1 low, and all other outputs high. Pin 1 of U5 drives

the arms of the two wafer switches for the Main Time Base selection low, as well as the arms of the Internal/External Time Base Selector switch and the Single/Dual Time Base selector switch. There are eight contacts in those addressed switches, six of them in the Main Time Base, Seconds 1 and 2, Decades 1, 2, 4, and 8, and one each in Single/Dual Time Base and Internal/External Time Base.

Six word addresses are required on the main frame front panel to interrogate all the switch contacts there, with the notable exceptions of the display oriented switches, cursor control switches, display expand switch, and Internal/ External Program Control switches. The display controls are only applicable to the visually observed display, and no purpose is served by remotely programming them. The Internal/ External Program swtiches are purposely front panel oriented to enable the operator to instantly verify instrument operation during those frustrating times when remote interface operation is being strived for, or when an interface failure may occur, regardless of cause, and the instrument integrity is suspect. There are two Internal/External Program swtiches that must be operated together to cause the control to change to External or to Internal. This feature strives to prevent the casually inquisitive individual from inadvertently changing status after a painstaking set up and data acquisition under External Program Control.

The Cursor Control switches are display oriented and their operation will be covered there, as will the Display Expand switch.

As may be seen, there are 46 contact points being interrogated on the main frame front panel by the use of four input signals and eight output signals. There are 15 test points available with installed turret terminals near the edge of the Front Panel PC Board making it possible to completely verify the operation of the multiplex system without probing a switch or a circuit. These are the six timed switch arm-drive signals, test points labeled A through F, and eight data output signals, 1 through 8, 1 being the least significant bit in the word and 8 being the most significant. A ground test point is the last one.

The front panel of the digital plug-in module has its switch contacts multiplexed in the same fashion as the main frame front panel. All switch contacts are so treated except for the termination selection switch for each data channel input and the eight Combinational Triggering data polarity selection switches. There are 28 contacts, requiring four time-multiplexed drive signals for the switch arms. On the schematic diagram for the 8201-D Front Panel PC Board, U1 through U8 are the eight multiplexer, or mux, circuits, and U9 is the binary four-line to ten-line decoder. The signal

R10PMADN8 is the most significant address bit in this case, making the times of selection of these switch arm drive signals mutually exclusive of those for the main frame front panel by virtue of the fact that this signal, R10PMADN8, is the complement of the signal R10PMAD8 used on the main frame front panel. There are 13 test points on the plug-in front panel PC board, located from the rear side of the board in the upper center of the board. Test points A through D are the four switch are drive signals, and test points 1 through 8 are bits 1 through 8 of the contact data words. The last test point is a ground.

A table of multiplex address assignments of each of the switch contacts on both front panels is included in the section dealing with the Remote Input/Output, as the individual contact addressing is identical in both cases.

Control Register

There are 96 flip-flops on the Control Register PC Board that are divided both logically and geometrically into two groups of 48 flip-flops each. One group is dedicated to storing the data pertaining to the condition of the switches on the main frame front panel, or to accept data through the Remote I/O to effect the desired remote control. Of these 48 flip-flops, 46 are used and 2 are spare. The other group of 48 flip-flops is used to store front panel data from the plug-in or from the Remote I/O to effect those control functions. Of the 48 flip-flops in the second group, 28 are used to store the necessary control data, and 20 have been reserved for future use in a possible option.

To consider the registers concerned with the storage of data from the main frame front panel, refer to sheet 2 of the schematic diagram of the Control Register PC Board. The data registers are each made up of four circuits of two flip-flops per circuit, all eight flip-flops being clocked by a clock pulse that has been gated with the decoded multiplexer address signal, identical to that signal used on the front panel to drive the selected switch arms. There are six such signals generated by the use of a 4-bit binary to ten-line decoder located at 14A, with its inputs driven by the same R10 PMAD signals as the front panel. These six signals are inverted by the circuits at 14B to make them positive signals, and are then each put into one input of a two input multiplexer packed four to a circuit, in 13D and 14D.

The other input to the multiplexer is driven by an identical signal generated by a binary to ten-line converter at 14C. The inputs to this circuit are called RI BUF SEL 1, 2, 4, and 8, and formed on the Remote Input/Output PC Board for the purpose of loading the Control Register via the interface from the external program control. To illustrate the routing of a single clock pulse, consider the instrument

to be in Internal Control or Front Panel Control. The control pins 1 of 13D and 14D are low, and PMAD signals are all low. The output pin 1 of circuit 14A is low, and 14B06 is high as is 14D11. All other data inputs to 13D and 14D are low. Because pin 1 is low on 14D, pin 11 input is selected instead of pin 10, and the circuit becomes enabled when pin 15 goes low. The signal RI0NCPCR, from the Remote Input/Output is Negative Clock Pulse to Control Register, and is low only for the last half of the time the PMAD lines are at one address. The output pin 14D09 passes the positive level through during the time of the clock pulse, which is then inverted by the circuit at 13E, output pin 6, and this is the negative clock pulse that clocks the register formed of circuits at 11A, 11B, 11C, and 11D on the positive edge of the clock pulse.

The data is gated through a group of two input multiplexers in two circuits at 13A and 13B. Thus, the eight data lines from the front panel are gated through these multiplexer circuits if pin 1 of 13A and 13B are low. If pin 1 is high, external input data is gated through. The outputs of the multiplexer circuits each drive the assigned bit of sic words of the Control Register. For example, the least significant bit output from the data multiplexer, 13B12, is connected to 11D12 (D input to LSB word A), to 12E12 (D input to LSB word B), 12D12, 15D12, 16E12, and 16D12. Each of the data bits is similarly connected. There are test points at the back edge, or access edge, of the PC board for the eight data bits, 1 through 8, and for each of distributed clock pulse lines, ADA through ADF, making it possible to probe the signals at D inputs and clock pulse inputs to all flip-flops on the board without extending the board to gain access to circuit pins. To verify flip-flop outputs, an extender board is required to gain access to the circuits or the PC edge connector pins.

The circuits on this half of the Control Register are duplicated exactly on the other half of the board. The signals that make the two halves of the board mutually exclusive are in the case of front panel control, the signal RI0PMAD8 used on circuit 14A12, and RI0PMADN8 used on circuit 4A12. For the case of external program control, the signal RI0 BUF SEL 8 is used on circuit 14C12, and RI0 BUF SEL N8 is used on 4C12.

7.25 Memory Address Control

The Memory Address counting and control is accomplished on the Address Control PC Board. The counter register size here for recording is 8 bits for a count of 256, which is exactly what is required by the memory devices used on the Channel Memory PC Boards. Addressing of the lesser significant 3 bits of memory for memory recall (display, plot, or digital output) is also accomplished on the Address Control PC Board. Referring to the schematic diagram for that

board, in the upper right corner, the two circuits at 15B and 14B are synchronous 4-bit binary counters, series connected into 8 bits, whose outputs are buffered and inverted for driving the address lines to the Channel Memories. These eight address lines are AD MADR 1 through AD MADR 8. The two circuits at 15A06 and 16A06 gate the MC Record signal to the Count Enable input pins 7 and 10 of 15B and pin 10 of 14B. That same signal drives the negative clear input to the least significant 3-bit counter circuit at 16B, holding it clear during recording and allowing it to count for recalling. The least significant 3 bits of this counter at 16B are combined by the gates at 16F11 and 16E11 to form a "carry" on count 7 to enable pins 7 and 10 of 15B through the gate at 16A input pin 5 for the memory recall address counting.

A holding register, called the End of Record address, using dual flip-flop circuits at 14C, 14D, 15C, and 15D, is used for storing the last address of each "Record," which is not necessarily the "overflow" address of the counter. This "last address" is caused to be loaded into this register by a signal from the Mode Control PC Board, MC STO ADR (Store Address) on two lines to reduce fan-out propagation delays. This signal occurs at the trailing edge of the "record" mode of operation, marking that address, the next being the first address of the record for starting display sweeps, plotting, or data outputting. Two binary magnitude comparator circuits, connected in cascade, at 15E and 14E, compare the contents of the memory address counter (15B and 14B) to the contents of the End of Record register. The "compare equal" output from this comparator, 14E06, is synchronized to the Memory Address Clock Pulse by the flip-flop at 12B. The output pin 9 provides the signal AD LAST MEM for stopping digital data output and for stopping data to the display, or for plotting until after flying back for a new sweep.

Displaying or Plotting, unexpanded, starts each sweep at the first address of the record. When the display and the plot are expanded, the output data to the display unit, or plotter, starts each at the position of the left Cursor, as will be explained in the section covering the Display Control. The Address Control PC Board has two "full binary adder" circuits, series connected, at 13C and 12C that add the most significant 8 bits of the Left Cursor Address to the 8 bits of the End of Record Address. The sum of this addition is presented to the "parallel data load" inputs of the Memory Address counter at 15B and 14B, and is loaded into the counter by a signal "N load cursor address" at pin 9 of 15B and 14B. The signal "N load cursor address" occurs during flyback of expanded displaying or plotting, as seen by the gates at 13D06, and 13E03.

At the bottom of the schematic diagram there are three of the lower frequency clock pulses, TB 2kHz PCP, TB 200 PCP,

and TP 20 PCP (2kHz, 200 Hz, and 20 Hz). One of these is selectable by jumper to connect to the inverter 12A05, whose output is used to drive a two-stage ripple counter at 13B. Another jumper selection at 13A makes it possible to select any plot clock pulse frequency in the 1, 2, 5, sequence from 5 Hz to 2 kHz. The gating at 12A02, 16A08, 16F08, 16E06, and 16E03 provides the plot clock pulse when plotting or provides the 2-MHz clock pulse for display sweeping at all other times, the resultant signal being called AD Sweep Positive Clock Pulse (SWP PCP). The and/or/invert gate at 16D provides the correct clock pulse to the Memory Address Counter in accordance with the mode instructions provided by the Mode Control PC Board. Address Clock Pulse, pin 2, and Record Mode, pin 3, provide clock pulses while recording. Display or Plot, pin 11, N Record, pin 12, Swp PCP, pin 13, and a large term concerned with flyback blanking, desplay expansion, character or data sweeping, provide clock pulses for displaying and plotting. Digital output mode, pin 4, and a "Timed Command" signal, RINTCMD, after inversion, on pins 4 and 5 provide clock pulses for addressing for digital outputting.

During the modes of recall of memory data, the Memory Address Clock Pulse at 16D08 is delayed through the gates at 16A03, 16C11, 16C08, and 16A11 to form a signal AD Read NCP to be sent to the Clock Generator PC Board for distribution to the Channel Memories for address register clocking. The N Record signal at 16A12 inhibits this clock pulse during data recording, when the Sample Interval Clock Pulse is used.

Display or Plot expansion clocking control is also done on the Address Control PC Board. Three signals, brought directly from the Front Panel PC Board, FPXDCN1, FPXDCN2, and FPXDCN4, are taken from the three contacts of the Display Expansion Wafer switch. The switch positions are 1, 2, 5 sequence, but the contacts are binary so that the following expansion factors carry the following output codes.

Xpand		
	X1	111
	X2	110
	X5	101
	X10	100
	X20	011
	X50	010
	X100	001

On the Address Control PC Board, these three signals are decoded by a binary to ten-line decoder circuit at 11C. Because the inputs are inverted polarity, the outputs follow a reverse sequence, with pin 9 being N Expand X1, etc. The

gating of terms to form the signal at 13E06 is "n flyback" and "display or plot expanded" and "data sweeps or plot sweeps." This signal enables the two decade counters at 11F and 12F, and resets the counter to zero when not enabled. Pin 9 on both decades of the circuits 11F and 12F is a negative synchronous parallel load input, with the parallel inputs grounded so as to load zero into both decades.

A negative "display or sweep clock pulse" is used to clock the counter up. After the counter has been set to zero, it will be counted up until the count matches the other inputs to the serially connected comparators at 11E and 12E. The "compare" output from 12E06, gated with "display or plot" in the gate at 13F11, and inverted by it, then parallel loads another zero into the counter. The signal out of the gate, 13F11, is AD N Disp Data Advance, also used on the Display Control PC Board. The "compare equal" signal from 12E06 is gated with the "expand," "displot," "N flyback" terms in the gates at 13F03 and 13F06. The other "or" term at 13F05 provides for continuous clock pulses when the expansion is X1. The output of the gate at 13F06 is 2-MHz clock pulses when in "display" and expand X-1.

When the expand is X2, every second clock pulse is gated through, allowing each memory data bit to fill two display data dots. When the expand is X5, every fifth clock pulse is gated through, allowing each memory data bit to fill five display data dots, and so on until at expand X100, each memory data bit is 100 display dots long or approximately 1/2 in. on a 5-in. CRT screen. The plot output signals are made to approximate the display signals (in X and Y) so all the expansion features, and other features, pertaining to the display are duplicated in the plot.

The coding gates and inverters at 12D and 11D are actually used to code a BCD number one less than the expansion factor because "zero" is a true count code not represented by an expansion factor. For example, for expand X5, a BCD 4 is presented to the comparator and the count sequence is 0, 1, 2, 3, 4 . Synchronous with the trailing edge of the 4, a new zero is loaded into the counter, starting the sequence over again, and the "data advance" clock pulse is created with the last half of the count 4.

7.26 Record Mode Control

Mode Control and Trigger Control

The Mode Control PC Board, with those portions of the Trigger Delay PC Board containing mode control, automatically sequences the instrument through recording, displaying, plotting, and digital outputting. It does this in accordance with the controls for Normal Triggering, Auto Triggering, Single Triggering, Delayed Triggering, Delayed Trigger Mode, Recording, Pretrigger Mode Recording, Manual Arm and Trigger functions,

whether these controls be derived from front panel status or external program stimulus. It also synchronizes these events to the clock pulses, whether they be internally derived or input from an external source.

Referring to the schematic diagrams, sheet two of The Mode Control Board, 0850-8201, and sheet two of the Trigger Delay Board, 0850-0311, it may be seen that the control of, and response to, Arming, Triggering, and starting and stopping of Recording in accordance with Trigger mode are all performed on the Mode Control PC Board. Near the upper left corner of the sheet, the three Trigger Mode Controls, Normal, Auto, and Single, are input to three inputs of a binary to ten line decoder. These signals are mutually exclusive, with one and only one being high at any one time. One output will then be low holding one of the two RS flip-flops at 12E, outputs at pins 4 and 9, set, or holding them both reset. Pin 12E04 is low for Auto Trigger, pin 12E09 is low for Single Trigger, and both are high with gate pin 13F11 low for Normal Trigger.

The normal sequence of events in the control of the 8200 starts with the Arm Ready function. This enables the Arm function to occur, which in turn sets Trigger Ready and starts Recording if Pretrigger Mode is selected and waits for Trigger to start Recording if Delayed Trigger Mode is in effect. When the Trigger Event occurs, Recording ends in Pretrigger Mode and begins in Delayed Trigger Mode to end when a full record of 2048 words is stored. If no other output is requested (i.e., Auto-Digital Output) when recording ends, the control advances to Display Mode, and Arm Ready is set to start another cycle. Any other output mode, Digital Output or Plotting, takes precedence over Display Mode, and the full record of data will be output through the Digital or Plot Output before the instrument is advanced to Display Mode and Arm Ready is set.

The Start Cycle flip-flop at 11D, output pins 8 and 9, is asynchronously set through pin 10 by the combination of signal in gates 14D06 and 16F06 such that N Record, N Trigger Ready, N Arm Ready, and not Pretrigger Mode Armed. The inverted output pin 8 of that flip-flop, through the inverter at 11A10 is one input, pin 9, to the nand gate at 13E. Another input, pin 10, is the signal TD Display Mode from the Trigger Display PC Board, where the Mode Control circuits having to do output mode control are located (output meaning any mode requiring memory output). Any other mode other than Display Mode will prevent Arm Ready, making it necessary to complete Digital Output, Plot Output, or Data Recording prior to enabling Arm Ready. The other input pin 13E11 is a large "or" combination of items that will cause Arm Ready. The combination of sweep address terms being input to gates 12A08 and 11B08 as well as the flip-flop at 14B, output pin 9, with the

term Auto Mode or Normal Mode at gate input 11B10, allows Arm Ready to be set only after one complete display cycle and at flyback time through the gate at 11C12. In single Trigger Mode, 11C05 is held high, 11C06 held low, and through 11B06, 13E11 is held high, allowing a normal sequence of events involving Arm, Trigger Ready, Trigger, and Record to be completed to enable setting of Arm Ready. The gate at 11B03 is used to provide an AD Last Memory pulse to set Start Cycle in the absence of a Display Control Board in the instrument, for trouble-shooting purposes. The output of gate 13E08 directly sets the Arm Ready flip-flop at 12E, "set input" pin 6. The output, pin 7, directly drives the D input of the Arm flip-flop 15E12, and the flip-flop will then be set by a positive edge signal at pin 11.

There are four signals that can cause Arm to be set. The inputs to the gate at 16F, pin 10, is Auto or Normal Trigger Mode, pin 9 is Neg. Single Trigger Mode and pin 11, which is Arm Ready, are such that is Auto or Normal Trigger Mode, the instrument is automatically "Armed" by the leading edge of Arm Ready, from pin 8 to the negative "or" inverting gate input 16C05, whose output drives the clock pulse input pin 11 of the Arm flip-flop. The External Arm input, after being detected and synchronized on the Trigger Delay PC Board, is sent via twisted pair to the Mode Control PC Board where it is converted from differential ECL level to TTL level by the converter circuit at 14A, input pins 2 and 3, as well as by output pin 4, which is then "or" connected at 16E13. The Arm signal from the front panel manual Arm switch via the control register is "or" input at 12D01. The "Arm Command" input from the Remote Input/Output interface through the remote status and command gating on the Trigger Delay Board is "or" input at 12D13. The composite term of these externally derived Arm signals at 16E11 is input to the nand gate 16E10, the control input term on pin 9 being Single Trigger Mode. Thus the instrument is externally Armed in Single Trigger Mode and automatically Armed in Auto or Normal Trigger Modes. The RS flip-flop at 12E, set pin 15, reset pin 14, is called "Armed." This name is a reminder that the Arm event has occurred and is set by the inverted output, pin 8, of the Arm flip-flop, which also resets the Arm Ready flip-flop through a RLC circuit delay of approximately 70 nsec at 14F. The output of the Arm Ready flip-flop feeds back to reset the Arm flip-flop, making the Arm event at the flip-flop output a short pulse of less than 100 nsec typically.

The output of the Arm flip-flop in Delayed Trigger Mode through the gate at 16D03 sets the Trigger Ready RS flip-flop, formed by cross-connecting two gates at 16C12 and 16D08. In Pretrigger Mode, the "and" gate 15F03, formed of Armed and Pretrigger Mode signals, drives the input pins 1 and 2 of the gate at 13E. The other input pin 13 is driven by the signal AD MADR OFL (Memory Address Overflow), ensuring that

one full record is recorded before setting Trigger Ready. The inverted output of the Try (Trigger Ready) flip-flop, 16D08, through the negative "and" gate 14D, input pin 13, with inverted Neg Outputting (Plot or Digital Output) in pin 2, which has been holding the Trigger flip-flop reset at 15E01, now goes positive to allow normal trigger action to set the flip-flop. The D input, pin 2, has been driven low for the period during which the Arm flip-flop was set, but is now high, waiting for a positive edge signal at 15E03 to set the Trigger flip-flop.

There are several sources of a trigger edge signal that may do this. One is the trigger input from the front panel External Trigger. This signal is combined on the Trigger Delay Board with the Combinational Trigger signal from the Digital Plug-in module. These two trigger signals are mutually exclusive, the desired one being selected by the position of the External/Internal trigger select switch on the front panel via the Control Register. The chosen signal is connected from the Trigger Delay Board to the Mode Control Board, over twisted pair as a differential ECL level signal. It is converted to TTL by the converter circuit at 14A, input pins 6 and 7, and output pin 5, which drives the negative input "or" gate 16C11. The trigger signal from the front panel Manual Trigger switch is input to the "nor" gate input pin 12D10. The Trigger "Command signal," from the Remote Input/Output interface through the remote status and command gating on the Trigger Delay Board, is input to the "nor" gate input pin 12D11, and that gate output, 12D08, drives the negative input "or" gate pin 16C10.

One more trigger signal source is the trigger pulser circuit, a flip-flop at 11D output pin 5 that is clocked at pin 3 by a 200-Hz clock pulse derived from the Time Base Board and inverted by gate 11E output pin 2. The flip-flop is normally held reset at pin 1 by the gate at 12D output pin 6. The purpose of this pulser circuit is to provide repetitive trigger signals in the Auto Trigger Mode, which is a "set up" mode, to force record and display cycling to enable the operator to verify channel data inputs and recording, threshold settings, time base selection, trigger delay settings, and the setting of all other pertinent controls.

The criteria of the inputs, pins 4 and 5 of the gate at 12D, to allow the pulser to output one trigger pulse, is that Trigger be Ready, pin 5, and Auto Trigger Mode be selected, pin 4. The gate at 13E inputs the Trigger Pulse on pin 5, the 200-Hz Positive Clock Pulse on pin 3, and the Auto Trigger Mode and Trigger Ready signal on pin 4 to output a trigger signal from pin 6 to the inverted "or" input pin 9 of the gate at 16C. The latch-up feedback signal on the Trigger flip-flop, from pin 15E06 to 15E04, holds the flip-flop set until the output through the nominal 40 nsec. RLC delay circuit

resets the Trigger Ready flip-flop through input pin 9. The inverted output, pin 8, then disables the gate input pin 14D13, and its output, 14D12, resets the Trigger flip-flop at 15E01. The Trigger signal thus generated is a nominal 40-nsec pulse used to start or stop recording, start the trigger delay counter, or change time base as the control settings require.

As may be seen on the schematic diagram, most of the gate input lines to the flip-flops controlling main or alternate time base, record mode, record end, and record stop are identified by a three or four letter abbreviation of the signal name. For the purpose of clarity, the discussion here of the signals concerned will be further identified. For example, one signal, Trigger flop, will mean Trigger flip-flop output rather than TD Trigger or the trigger signal from the Trigger Delay PC Board.

The Main/Alternate time base flip-flop is held off at 13C13, preventing Alternate Time Base selection for Single Time Base mode (14D09) or for External Time Base (14D10), when not recording (15D09), during Record End (15D10), and during data Output Mode (15D11). The Dual Time Base (Main/Alternate Time Base) flop is enabled by Dual Time Base (14D09) and clocked to Alternate Time Base by "any delay count remaining" (TDN CNT Ø - 14E05), Pretrigger Mode (14E04), and Trigger flip-flop (14E03), or by Dual Time Base (14E02), Delayed Trigger Mode (14E01), and Trigger Delay Counter reaching 0 count (14E13). The Main/Alternate flip-flop output pin 13C08 carries the significance of high level for Main Time Base.

The Record flip-flop is an RS flip-flop formed by cross connecting the two gates at 15C08 and 15D08. This flip-flop may be set by Pretrigger Mode (15D03), Arm flop (15D05), Not Output Mode (15D04), Delayed Trigger Mode (12A01), Single Trigger Mode (12A02), the End of Trigger Delay pulse (12A04, 05) Single Trigger Mode (15C05), Delayed Trigger Mode (15C04), Trigger flop (15C02), Trigger Delay counter at Ø (15C01), Delayed Trigger Mode (15D01), Dual Time Base (15D02), Trigger flop (15D13), or by Arm flop (15D05), Pretrigger Mode (15D03), and Not Outputting (14D04). The Record flip-flop can be reset by a change of mode to Output Mode (15D11) or by a negative level on the N Record End flip-flop output 14B05.

Two Flip-flops at 15B, N Record +1, and N Record +2, follow the Record flip-flop in shift register fashion, synchronized to the free running 20-MHz N clock pulse at 15B03 and 15B11 clock pulse inputs. The N record +2 flip-flop output 15B08 holds the N Record End flip-flop (14B04) until Record +1 becomes active, raising 14B04. Prior to the Record flip-flop being set, the End RS flip-flop, formed by the cross-connected gates at 12C08 and 12B11, has been held off by the Record flop at 12B13. This flip-flop may be set at the end of recording by Record +1 (12C01), Pretrigger Mode (12C04), Trigger flop (12C02), Trigger Delay counter at 0 (12C05),

Record +1 (13D11), Pretrigger Mode (13D10), End of Trigger Delay Count (13D09), Trigger Not Ready (16F02), Record +2 (15F04), Pretrigger Mode (15F05), End of Trigger Delay count (15F10), not Armed (15F09), or by a remote input through the status and control gating on the Trigger Delay Board from the Remote Input/Output interface. As may be seen, the main purpose of the End flip-flop is to cause an orderly "halt" in the Pretrigger Mode recording, with or without a Trigger Delay Count. The inverted output of the end flip-flop drives the input pin 1 of the negative input "or"gate at 13B, whose output pin 3 drives the D input of the stop flip-flop at 13C, which is clocked by the Memory Address Clock pulse and buffered by two gates at 12B03 and 12B06. The inverted output of the stop flip-flop, pin 4, is fed back to the gate input 13B02 to hold the flip-flop set until it is asynchronously reset by the Record +1 flip-flop setting at the ends of Record Mode. In Delayed Trigger Mode, the record length is just one full record, starting at address 0, so the stop flip-flop is set by the gate output 13D12, whose inputs are Delayed Trigger Mode (13D13), Ad MADR OFL (13D01), and Memory Address Clock Pulse (13D02).

The inverted output of the Stop flip-flop, 13C06, drives three negative input "or" gates, pins 13B05, 13B09, and 15A09. The other input of each of these gates is driven by the same signal as the direct set input of the Stop flip-flop from 13D12. These three gates provide three identical signals for fan out and to minimize propagation delay, or Store Address 1, 2, and 3. Two of these signals are used to clock the contents of the Memory Address Counter into the last address register on the Address Control PC Board, and the third one is used on the Clock Generator PC Board to stop record clocking functions. One of these gate outputs is used in a gate at 13B12 with the reverse phase of the record clock in 13B13 to create a reset signal for the RS flip-flop formed by cross-connecting the gates at 14C03 and 14C06. The set input 14C01 is normally held low until Record +1 goes high and stays high during recording. When the Stop flip-flop is set at the end of recording, the RS flip-flop at 14C is reset through pin 5. The output pin 3 goes low enabling the N Record End flip-flop to be reset by the Negative Record Clock pulse at 14B03, and the output 14B05 goes low, resetting the Record flip-flop through pin 15D10. N Record +1 and N Record +2 are then set in sequence, causing the Stop flip-flop to be reset, the RS flip-flop at 14C to be set, and N Record End to be set.

Two gated signals are provided by the use of a 40-nsec RCL delay circuit at 16A to delay the signal from the N Record output, with respect to the Record output, and to provide a nominal 40-nsec negative pulse from the gate at 16A06, which occurs at the start of recording to clear the Memory Address Counter to zero on the Address Control PC Board. This same pulse signal is inverted by the gate at 16B02 to be used to reset the Time Base decade counter at the beginning of

recording to reduce the jitter in position of change of time base when in Dual Time Base Mode. Several other gates are used on the Mode Control Board to buffer and/or invert output signals such as MC Record Gate, MC Negative End of Record (MCNEOR), MC N Arm Event, MC Arm Ready, MCN Arm Ready, MC Trigger Ready, MC N Trigger Ready, MC Trigger Event, and other mode status signals.

Trigger Delay

The Trigger Delay counter circuits are located on the Trigger Delay PC Board, as are the External Arm and External Trigger input circuits. The External Arm and External Trigger input circuits are identical to the Data Input circuits, each one having a relay controlled selectable input termination bit K1A and K2A, and a differential FET "source follower" pair to provide an input voltage rating of ±50 VDC at Q6 and Q7. This drives the inputs of a high-speed differential comparator at 1AA and 3AA, which drives the gating and flip-flops in a latching circuit at 1A-B, 3A-B, 1B, and 3B as seen on sheet 1 of the Trigger Delay schematic diagram.

The similarity stops here, because the Arm and Trigger input circuits have only the latching connection. Also, the series connected string of flip-flops is four long instead of two long, and are formed by the flip-flops at 1B and 1C for Arm and by those at 3B and 3C for Trigger. After the first flip-flop or latching flip-flop in each string, the remaining three are clocked by the Sample Interval Clock Pulse derived from the Clock Generator Board, and buffered by the gate at 2B input pin 6. Outputs of the second and third flip-flops in the Arm circuits, pins 1B02 and 1C15, through the "nor" gate at 1D05 with the inverted output of the last flip-flop in that string, 1C03. This stretches any received positive pulse or positive edge into a two Sample Interval wide signal. The Arm Polarity control signal at the converter circuit 2F05 is converted from TTL to ECL level and inverted to control the gate input 1D07. The gate output, pin 3, then is a two Sample Interval positive pulse and is emitter "or" tied with the output pin 14 of 1D of the gate that decodes the negative pulse or negative edge of the Arm input. This then drives the input pin 4 of the balanced line driver at 2D, which drives the balanced External Arm signal through twisted pair to the Mode Control board.

The Trigger circuits are duplicates of the Arm circuits, with the four flip-flops at 3B and 3C, the two "nor" gates at 2B14 and 3A-B15, the two negative input "and" gates at 3D03 and 3D14, and the balanced line driver at 2D outputs at pins 6 and 7. One difference in the Trigger circuits is the input of the Combinational Trigger signal into the first flip-flop of the string. After being buffered and inverted by the gate at 3A-B14, it is used to drive the D input of that flip-flop.

The External/Internal Trigger control signal, after being converted from TTL to ECL level by the circuit at 2F15, is applied to the control clock input pin 6 of the flip-flop at 3B.

The Sample Interval Clock pulse is on pin 9, which is common to both flip-flops in the circuit at 3B. When pin 6 is held high (External Trigger), the clock pulsed on pin 9 are blocked from the flip-flop whose D input is pin 7, but not blocked from the flip-flop whose D input is pin 10. When the clock input pin 6 in held low (Internal Trigger), the clock pulse on pin 9 is allowed to clock the data on pin 7 into the flip-flop. The Internal Trigger control also causes the two gate outputs, 2A02 and 2A03, to be high. These outputs are emitter "or tied" to the outputs of the Trigger comparator circuit at 3A-A, which in turn is the inactive state for the inputs of the two latch gates, 3A-B02 and 3A-B03.

The Trigger Delay counter uses three series-connected 4-bit BCD ripple up/down counter circuits, which in this application are counted only down. In addition, the circuits are capable of being asynchronously parallel loaded with the data on the parallel inputs by the negative "load enable" signal being applied at pin 11 of each of the counters at 6D, 6C, and 6B. The signal used in the Trigger Delay counter circuits is N Arm Event from the Mode Control Board. The data loaded at that time are the three decades of BCD data held in the Control Register flip-flops corresponding to the contact signals derived from the Trigger Delay Selection lever switches through the panel signal multiplex system, or corresponding to the External Program control signals from the Remote Input/Output Board through the remote interface.

The Arm Event signal loads the delay setting data into the counter, the Trigger Event signal opens the control gating, and the counter is counted down by a clock pulse signal that is 1/10 the repetition rate of the Sample Interval. When the counter reaches zero, the clocks to the counter are gated off, and an "end of delay" signal is sent to the Mode Control Board causing Delayed Trigger action.

The ECL 4-bit decade counter at 4D counts the Sample Interval Clock pulse down by a factor of 10. Its output, pin 12, is converted from ECL to TTL by the circuit at 4E04. That signal is then gated at 5A11 with a signal on pins 5A09 and 5A10 from 6F11, which is high any time the content of the counter is not zero. Thus, the clock pulses are gated and inverted at 5A08 to supply clock pulses to the counter string at 6D04, and to a flip-flop at 5E11 until the counter counts down to zero and clock gate at 5E08 is shut off. The flip-flop at 5E output pin 8 operates in parallel with the least significant bit in the counter circuits. The propagation

delays in the counter circuits are too long when being counted at the fastest rate (20 MHz) to provide a synchronized "end of count" signal to effect an orderly shut down of the counter, so a higher speed device is used to logically replace that least significant counter bit. That flip-flop is asynchronously set at 5E10 by the Arm Event gated with the CR TRG DLY 0.01 signal, just as is the least significant bit of the counter by the gates 5F11 and 5F08.

The flip-flop at 5E, clock input pin 3, is clocked by the free-running 20-MHz clock pulse. Its D input pin 2 is driven by the Turn On Power Clearsignal (as is the clear input of each counter circuit). This provides an output, pin 6, which asynchronously clears the other flip-flop at 5E1B. The gate at 5A0C and the two flip-flops at 5B provide a signal at 5B06 that, with the delays and conversion of L1, C88, and 2F14, synchronously release the decade counter at 4d at the beginning of the Trigger Delay count-down. The Trigger Event, through the gate at 5A12, asynchronously sets both flip-flops at 5B. The output 5B08 goes negative, which shuts off the gate at 5A13 to be negative approximately 10 nsec. Both flip-flops remain set because the first D input, 5B12, stays high until the count-down reaches zero, 6F11 goes low, the next clock pulse clocks 5B09 low, the next clock pulse after that clocks 5B05 low, and 5B06 goes high.

The two flip-flops at 6E are used as an "edge detector" to shift in the negative edge signal from 6F11, which is also inverted at 5D02. The low signal at 6E02 is shifted to 6E12 by the first clock pulse on pin 3, and on to 6F10 by the second clock pulse. The signal out of 6F08 is a negative pulse nominally 75 nsec wide, synchronized at the trailing edge to the 20-MHz clock pulse.

The control circuits for the various output modes are located on the Trigger Delay PC Board and are illustrated on sheet 2 of the schematic diagram for that board. Several other circuits are located there because of space availability and will be included in this section.

The upper left corner of this diagram shows the logic for decoding the no-op positions of the Time Base selection switches, which are actually capable of being positioned to indicate time bases from 0.1 nsec to 50 sec in the 1, 2, 5 sequence. Time bases are electrically selectable only from 5 nsec to 5 sec. The no-op codes are then 0.1 nsec, 0.2 nsec, 0.5 nsec, 1.0 nsec, 2 nsec, 10 sec, 20 sec, and 50 sec for both Main and Alternate Time Bases. The no-op decode logic is required to drive front panel indicators to inform the operator of a non-functional time base selection as a clue to the cause for an apparent total failure of the instrument. When an illegal time base is selected, no clocking functions occur for recording.

As may be seen, the logic for Alternate Time Base no-op is a duplicate of that for the Main Time Base. The output pin 8 of the gate at 11A is true for any selection 0.1 to 20 nsec. The inverter output 11C08 is true for selections 0.1 to 1 of any range. The output of the gate at 11B06 is low for any selection 0.1 to 1 nsec, making the inverter output 11C10 high for those selections. The gate output 11B08 is low for any selection 2 to 20 nsec, and the gate input 11A02 is low for 0.1, 0.2 2, 5 and 50 of any range. The input 11A13 is low for 0.1, 0.5, 2, 10 and 50 of any range, so the gate output 11A12 is true for the one selection, 2 nsec. The gate output 11D03 is true for the seconds range. The inverter output 11C12 is low for a selection of 50, any range, and the gate output at 11B03 is low for selection 10 and 20 of any range. The gate output at 11B11 is true for 10, 20, and 50 of any range, and the gate output 11D11 is true for 10, 20, and 50 sec, making the output of the gate at 11A06 low for any of the no-op selections, 0.1 to 2 nsec and 10 to 50 sec.

A power turn-on reset pulse is generated on this board by the use of an RC network, R100 and C78, which provides a rising exponential waveform with a time constant of nominally 0.022 sec. This signal is buffered by the transistor Q5 followed by a Schmitt inverter circuit at 13B output pin 10 and a power buffer at 12A03 to provide a Negative Power Clear. That signal is also inverted again by another power inverter at 12A06 to provide a positive Power Clear signal. These two signals are used to clear various registers, counters, and control flip-flops to prevent their being initialized to a random configuration at power turn on.

There is a group of gates in the lower center of the schematic diagram that accepts a command input word from the Remote Input/Output Board through the Remote Interface that makes it possible to independently Arm, Trigger, Reset Record Mode, or Reset Output Mode (Digital or Plot). These gates decode the appropriate input signals and control signals, the various gate outputs being 13D11, 16D11, 16D06, 16B06, 15A08, 16B12, and all 8 gates at 13A and 14A.

The Digital Output Mode is basically controlled by a serial string of three flip-flops. Digital Output Mode is at 14B09, Digital Mode Cancel is at 14B05, and Timed Digital Output is at 15C09. Any Digital Output command, either front panel or remote input, will, with the positive edge through the gates at 12A11 and 12A08, clock the flip-flop Digital Mode on at 14B11, provided a Record Mode is not in process holding the D input low at 14B12. Output 14B09 will go high and 14B08 will go low, to satisfy the criteria of the gate at 14C11, which in turn causes 15C12 to go high and the trailing edge of the next AD Last Memory Address signal to set the Timed Digital flip-flop. The output pin 15C09 goes high disabling the gate input pin 14C09 until another complete cycle

is achieved. The output pin 15C09 also enables gate input 13D10, while the other input pin 13D09 is already enabled by the output pin 14B09 of the Digital Mode flip-flop. The gate output 13D08 now enables the D input pin 14B02 of the Digital Mode Cancel flip-flop. A second request for Digital Mode will set the Cancel flip-flop, which at gate input 15B03 will cause the gate output pin 6 to reset the Timed Digital flip-flop. The Timed Digital flip-flop's output pin 8, through the inverters at 16C12 and 16C10, drive the input pin 2 of the edge detector gate at 15B, and its output, pin 8, resets both flip-flops at 14B. Thus, the method of cancelling a Digital Output, without waiting for a normal completion, is to make a second application of the manual Digital Output front panel switch or to request a Digital Output through the Remote Interface. The normal completion of the Digital Output Mode is at 15C11 by the AD Last Memory Address pulse, indicating that the entire contents of memory have been output.

The Plot Mode controls are almost identical to those for the Digital Output Mode. The three serially connected flip-flops for Plot Mode control are Plot Mode, output at 14D05, Plot Cancel at 14D09, and Timed Plot at 15C05. The CR Plot Out signal drives the clock pulse inputs to both flip-flops at 14D. For any mode other than Record Mode, 14D02 will be high, and the positive edge of the Plot Out signal will set 14D05 high, and also gate input 13C01. If 13C02 is high, the instrument is in Digital Output Mode, and Plot Mode will wait for completion of Digital Output Mode. If 13C02 is high, or when it does go high, 13C03 will go low, and drive 14C03 low. As for the other pins, 14C04 will be low, 14C05 will wait for DC Sweep Address 4, and the same signal latched by the flip-flop at 14E09 will agree to enable the D input to the Timed Plot flip-flop 15C02. Sweep Address 4 starts the plot output, thus eliminating the plot of the first eight sweep cycles concerned primarily with the characters for display. The plot may be cancelled at any time by premature resetting of the flip-flop at 14E09. The Timed Plot flip-flop is synchronized to the AD Sweep clock pulse, inverted by the gate at 12D11. Recalling the clock gating on the Address Control PC Board, in Plot Mode the Plot Clock Pulse is used to clock the Memory Address Counter and the Display Sweep Address Counters maintaining synchronization in the instrument. Plot Mode, like Digital Output Mode, can be cancelled by a second request for Plot Mode while in Plot Mode. Both gate inputs 13D04 and 13D05 will be high, and the D input to the Plot Cancel flip-flop 14D12 will be high. The positive edge of Plot Out at 14D11, causing 14D09 to go high, disables the gate input 14C04 and enables the gate input 15D03, causing the output 15D06 to reset the Timed Plot flip-flop. The inverted output 15D06 which goes high through inverters 16C02 and 16C04, will cause the edge detector gate at 15D12 to provide a narrow pulse at 15D11. That gate output, pin 8, will reset the Plot Mode and Plot Cancel flip-flops.

The Plot Pen controls are enabled by DC Pen Enable, which is a signal corresponding to just the data portion of a normal display without characters, without flyback, and with the eight data channel sweeps. This signal at the D input to the flip-flop 11E02 is synchronized by the Sweep clock pulse at 11E03. The flip-flop output 11E05 is gated at 12D02 with the Pen Enable signal at 12D01, and the gate output direct resets the flip-flop at 11E13. The Signal DC2047 is a "one clock time" wide pulse occurring during the next to last clock time of every sweep, each sweep being 2048 counts, or clock times, wide, with a 16 count flyback. The flip-flop at 11E11 is clocked by the Sweep clock pulse, The sense of this flip-flop output pin 8 is high for "pen up."

The cycle starts at the beginning of a data sweep by 11E02 going low, one clock later 11E05 goes low, ending the pulse to reset the flip-flop at 11E13. This causes 11E08 to go high, enabling the gate at 13D02, whose other input is enabled by Plot Mode. The output pin 13D03 also goes high, driving the inverting buffer gate 16D10. When DC Pen Enable goes high near the end of the sweep, the flip-flop clock input 11E11 sets the flip-flop. The output pin 8 holds the flip-flop set at pin 10 until the next sweep starts, and the pen is lifted and held up until that next sweep starts.

The signal at 15A01, MC Negative Memory Address Clear, occurs at the start of each Record Mode. It is gated, at 15A02, 04, and 05 with Negative Power Clear. The gate output 15A06 is then used at 15B05, 15B10, 15D05, and 15D10 to cause Digital Output Mode or Plot Mode to be terminated when recording starts and to be cleared at Power Turn On.

When the signal CR Normal/Auto Digital is low, signifying Automatic Digital Output Mode on completing each Record Mode, that signal is gated at 16B09 with the signal MC Negative End of Record (MCNEOR) at 16B10. The gate output, 16B08, through the inverter at 13B08, asynchronously sets the Timed Digital flip-flop. The Digital Output Mode will be terminated normally by the AD Last Memory signal, inverted and applied to 15C11. Or it may be terminated by two successive Digital Output requests, thus allowing the Digital Mode and Digital Cancel flip-flop to operate the Cancel logic.

7.27 Input Threshold Voltage Selection

The Input Threshold Voltages are selected by position of the Threshold Voltage lever switches on the plug-in module front panel. There are two voltages selectable, Threshold A and Threshold B. Each voltage is controlled by a combination of three lever switches or wafers. Each wafer outputs a two line, three line, or four line BCD code representing the position of that lever. The following chart shows the correspondence between selected position and output code for each of the three wafers.

Volts	BCD Code	Tenths	BCD Code	Millivolts	BCD Code
+2	0000	0	0000	0	0000
+1	0001	0.1	0001	0.025	0001
+0	0010	0.2	0010	0.050	0010
-0	0011	0.3	0011	0.075	0011
-1	0100	0.4	0100		
-2	0101	0.5	0101		
		0.6	0110		
		0.7	0111		
		0.8	1000		
		0.9	1001		

In the cases of the volts wafer and millivolts wafer, the unused most significant bits are shown here merely to illustrate the switch coding and are not included in the decoding logic. As may be seen on the Schematic diagram for the Mode Control PC Board, sheet 1, the two Threshold voltages are generated by digitally driven digital-to-analog converters. By the use of a BCD to ten-line converter at 1A, the six individual states of the volts wafer are decoded to single lines. They are then combined in gates to form the terms - sign at 1C08, +2 or -2 V at 1B11, +1 or -1 V at 1B08, and +0 or -0 at 1B06.

Because the switch outputs are BCD coded, and because the most desirable Digital-to-Analog Converter (D/A Conv. or DAC) is one that uses binary-weighted voltage-driven summing node components, a series connected pair of 4-bit binary-full address circuits was used at 3A and 2A to accomplish the BCD to binary conversion. The D/A converter is symmetrical, folded out at 0 V by the sign bit. Hence the technique used to convert BCD to Binary coding was merely to subtract binary difference between the switch generated BCD code and the binary code required for the voltage desired. The 25-mV increments coded by the least significant wafer of the switch are already a binary extension of the tenths wafer, so no further coding is required there. The BCD progression from 0.9 to 1.0 causes a jump in the binary code equal to 0.6, and so, between 1 V and 1.975, 0.6 binary is subtracted from the input code (actually implemented by adding

the bit complement +). And, between 2.0 V and 2.975 V, 1.2 in binary equivalent is subtracted (again implemented by adding the bit complement +1). So, the binary code to be added to any BCD number starting in 1 is 11001000, disregarding the sign bit, and for any number starting in 2 is 11010000.

There are eight signals of the binary adder circuits at 3A and 2A representing the combination binary-BCD codes selected by the switches, and a ninth signal, the sign, which symmetrically folds the binary code about zero. The exclusive "or" circuits at 2B and 3B are used as a sign control inversion for + sign, non-inverting for - sign, and buffers, which in turn drive the open collector inverters at 2C and 3C. To consider the inverter output at 2C08, resistor R2 and potentiometer R60 form a nominal 13 kΩ connected to +15 VCD when R60 is centered. When the inverter output at 2C08 is high and supplying no current to or from the node, the current flowing from +15 V flows through CR2 and through the parallel pair of resistors R20 and R30 to ground essentially.

The reference voltage at pin 3 of the summing operational amplifier at 2F-B is ground, so the summing node at pin 2 is nominally at ground to considerably greater accuracy than the resolution of this D/A converter. With the voltage across R20 and R30 equal, the current through them is inversely proportional to the ratio of their resistance values. R20 carries approximately 1/2 mA to the summing node, which must be taken out by the feedback resistor combination R61 and R63. The voltage value required at the amplifier output to compensate the input current from R20 is 3.2 V (and Ohms Law) which fixes a combined value to R62 and R63 of 6.4 kΩ, so that the setting of R63 will nominally be at 780 Ω.

When the inverter output at 2C08 is low, that voltage is nominally less than 0.2 V, reducing the forward voltage across CR2 to that voltage because essentially no current flows in R20 and R30. At this voltage, the current through CR2 is typically less than 1 μA, and so the current error at the summing node is less than 1/4 that contributed by the least significant bit of the D/A converter.

The current to the summing node is controlled in this same way for each bit in the D/A converter. The summing node resistors for currents from each of the bits R29 through R37 for the bits, sign through 0.01, respectively, are binary increasing values from 1 kΩ for the sign, to 261 kΩ for the 0.01 bit. Each summing resistor to the summing node is paralleled by a resistor to ground, of such value that the parallel equivalent of the two resistors is approximately 1 kΩ, as seen by the input diode and pull-up resistor for that bit. The current switched by the open collector inverter in each bit input is nominally 1 mA. The pull-up resistors for the two most significant bits, the sign and 3.2 bits, are trimmable by the use of potentiometers R59 and R60 to reduce the component accuracy requirements for those two bits.

Another potentiometer R62 with resistor R28, take a current from the summing node equal in magnitude to that inserted by the sign bit input components. This causes the D/A converter output to be from +2.975 V to -2.975 V rather than from 0 V to -5.950 V, as would be the case if all currents into the summing node from the binary bits were "into the node-plus to minus."

The output of the summing amplifier 2F-B06 drives a buffer follower amplifier at 2F-A to provide a dedicated driver circuit for the comparator circuit loads throughout the instrument.

The Threshold A D/A converter circuits are exactly duplicated to provide the second, Threshold B D/A converter output buffer, input encoder and BCD to binary encoding logic, as seen on the lower portion of the schematic diagram. The +15 V and -15 V power supply filtering components, L1, L2, C15, C16, C17, C18, R81, and CR19, are shared by both D/A converters.

Another part of the threshold selection logic is located in the plug-in module, mounted on the bottom strengthening panel. Another printed circuit board, called the Threshold Selector PC Board, contains the analog switching circuits for each of the input channel comparator threshold inputs. The choice for each channel is for either Threshold A or Threshold B to be applied to the threshold input of its comparator. The top portion of the schematic diagram, 0850-296, shows the switching circuits for Channel 1. Two operational amplifiers at U-6 are connected to the signal CR1T-A/B, which is from the Control Register, Channel 1 Threshold A/B. When this logic signal is high, Threshold A is to be connected to the Channel 1 comparator, and when the signal is low, Threshold B is to be connected to the Channel 1 comparator. The amplifier at U-6 output pin 1 is connected as a full-gain saturating noninverting amplifier, and the amplifier U-6 output pin 7 is connected as a full-gain saturating inverting amplifier. A logic mid-point voltage is generated by the resistor diode string R17, CR18, and CR17. This is nominally +1.75 V and is connected to pin 2 input of the noninverting amplifier and to pin 5 of the inverting amplifier. These amplifiers saturate without latch-up, at about +13 V or -13 V, depending on the input polarity selected, but the two amplifier outputs are complementary for any given signal.

Consider CR1T A/B to be low, selecting Threshold B to be connected to the Channel 1 comparator. Amplifier output pin 1 will be at -13 V, and through diode CR1 holds the field-effect transistor Q1 biased off at the gate, pin 3. The source, pin 1, of this transistor is connected to the Threshold A, as buffered by the follower amplifier U3 output pin 1. The drain, pin 2, of Q1 and the drain of Q2 are connected to a buffer follower amplifier U1 output pin 1, which drives the comparator input of Channel 1. Because Q1 is turned off, the drain of Q1 is in the

high impedance state or open circuit. At the same time, U6 pin 7 is at +13 V, back biasing CR2, and Q2 is driven on by the resistor R2 from the source voltage for Q2, which is Threshold B. Threshold B has been buffered by the follower amplifier U3 output pin 7. The gate of Q2 is essentially at the same voltage as the source, and Q2 is on or at a very low impedance between power and drain so that Threshold B is applied to the buffer follower amplifier, U1, input pin 3.

This same set of circuits is repeated for each of the eight channels, except for the buffer followers U3. Each follower amplifier at U1, U2, U4, and U5 has a bypass filter capacitor at its input to cause each output to be essentially a ripple-free duplicate of the Threshold voltage selected.

7.28 Output

Digital Display

The display signals for the 8200 are totally digital and synchronous including the sweeps, the channel raster, the character display, and the cursor display. This makes it possible to create horizontal display expansion factors of up to 100, with precise marking by the two cursors provided and without display jitter that is sometimes found when large magnification factors are applied to multivibrator generated sweep circuits.

The schematic diagram for the Display Control PC Board, 0850-0316, is on two sheets. Referring first to sheet 2, the foundation for the entire display or plot system is the series connected set of five synchronous binary counters at 11D, 11F, 12F, 13F, and 14F. Remembering that the AD Sweep Positive Clock Pulse is a 2-MHz clock pulse for displaying and a plot rate clock pulse for plotting, selectable from 5 Hz to 2 kHz, the sweep clock pulse is inverted at 13D12 for use by the counters and buffered at 11A11 for use by the negative-edge triggered J-K flip-flops at 11B01, and after some gating at 12B01, 12B13, 13B01, 13B13, and 11B13. The counter at 11D is a 4-bit binary counter used only to count 16 counts for each trace fly-back. The flip-flop at 11B, outputs at pins 5 and 6, is used to control flyback and blanking functions.

For this discussion, only the Display Mode will be described. Remember that for plotting, only the clock pulse rate from the Address Control PC Board will be reduced, and so all the events occur at the reduced rate.

When the Display Mode starts, the signal TD Displot Mode goes high, having been low to hold off "and" gate inputs 11C01, 11C10. It was also low to hold off the negative "or" input low at 11C12 and the Flyback flip-flop reset at 11B15, its output 11B05 being low. Then TD Displot Mode and gate output 11C08 go high, enabling the counter inputs 11F07, 10. Counting up occurs

on the trailing edge of each negative sweep clock pulse. Only the least significant three bits of this counter are used, these being gated together for count 7 through gates 11A03 and 11A06. This count is then used to "carry enable" the counter at 12F10, the other enable 12F07 having been enabled by the signal from 11C08, as was 13F07 and 14F07. The "carry" out of 12F15 is used to enable the "carry input" to 13F10, bringing the total number of binary counter bits at this point to 11 for a total count of 2048. The "carry out" at 13F15 in addition to being fed forward to 14F10 is also used at the J input, 11B03, of the flyback flip-flop causing it to set on the negative edge of the next clock pulse. Output 11B05 goes high causing 11C03 to go high, enabling pins 11D07 and 11D10 of the flyback counter, while 11B06 goes low causing 11C08 to go low, disabling the counter string 11F, 12F, 13F, and 14F. The same clock pulse that set 11B05 high also advanced 11F, 12F, and 13F to zero and advanced 14F to a count of 1, making 14F14 go high and the first sweep, Sweep Ø, to be completed.

The flyback counter now counts to binary 15. When its overflow 11D15 goes high, driving 11B02, the next clock pulse will reset the flyback flip-flop. The second sweep starts after 11B06 goes high, 11B05 goes low, the flyback counter 11D is disabled, and the sweep counters 11F, 12F, 13F, and 14F are enabled. There are 16 sweeps numbering 0 through 7 and 10 through 17 using octal notation. For the purpose of clarity, there are 2048 incremental positions in the sweep (the total count of the eleven Sweep Address counter bits) and these eleven signals are called Display Address 0 through Display Address 10. The 16 sweeps are counted by the four Sweep Address bits, called Sweep Address 1 through Sweep Address 4. Sweep Ø is used to update the Decimal Difference Counter located on the Cursor Control PC Board, which is then left in that count state for the character display, not being updated until the next Sweep Ø. After Sweep Ø, the next seven sweeps are used to trace the seven rows of dots for the character display. The last eight sweeps are the data sweeps, one for each of the eight data channels, which are swept, Channel 1 through Channel 8, from top to bottom All of the data of Channel 1 is displayed, first bit on the left side through the last bit on the right side before flying back to start Channel 2 and so on.

The analog sweep voltage for driving the display is generated by converting the eleven Display Address Counter outputs through a D/A converter. Each of the counter outputs is buffered by a dedicated inverter circuit, open collector type, at 15D for the least significant 6 bits, and totem pole output type at 15E for the most significant 5 bits. The summing operational amplifier at 16A-A has its reference input, pin 3, nominally held at ground, so the summing node pin 2 will nominally be at ground for all input conditions of the input bits.

To consider the current switching that occurs in the most significant bit, Display Address 10, assume first the case where 15E02 is high, supplying current through CR49 to hold R161 high enough to back bias CR44. This requires about 6 mA. The positive current source formed by the series combination of R155 and R151, with the summing resistor R126, total about 14 kΩ, and with the voltage drop in CR39, will pass approximately 1 mA to the summing node. The summing resistor R126 is paralleled by a resistor, R146, of a value such that the parallel combination is nominally 1 kΩ. The impedance at the input to each summing resistor in the D/A converter is nominally matched to each other, causing the current through each of the diodes driving the summing resistors in the "on" state to be nominally 1 mA. When the inverter output 15E02 is low, the current in R161 now pulls down the current source resistors R155 and R151, causing CR39 to be nominally zero-biased, or zero-voltaged, and no current is supplied to the summing node through this bit. The most significant 5 bits of the converter are identical, except for the resistance value of the summing resistor and its impedance matching resistor. The resistor has a potentiometer in each current source leg to allow adjustment to compensate for initial component tolerance. The least significant 6-bit inputs are driven by the open collector inverters at 15D not requiring the switching diodes and pull down resistors.

The feedback loop around the amplifier R111 and potentiometer R110 make it possible to adjust the voltage gain of the amplifier such that the output voltage swing is nominally 2 V. The offset resistor R114 provides a current equal and opposite to the most significant bit input, and the amplifier output swings symmetrical about 0 V. The output is buffered by two dedicated analog voltage follower circuits at 16A-B, one to drive the Display Unit Horizontal input through the 2:1 attenuator R108 and R107, and the other to drive an external display through the attenuator R109 and R106. In addition, the buffer output 16A-B-01 drives the "Plot X" output through a current limit resistor R112 without attenuation. The FET transistor Q23 acts as a grounded source switch to ground that output when not in the "Plot Mode." When the signal MC Plot Mode goes high, R113 pulls the base of Q22 high, turning Q22 from "on" to "off." Its collector, which has been near ground, is now pulled negative by R129, which also drives the gate of Q23, turning it from "on" to "off." The "Plot X" output now becomes active.

The BCD to 10-line converters 11E, 12E, and 13E are used to decode the most significant 8 bits of the Display Address Counter into three sets of lines representing octal code counts of the counter. In other words, the second least significant 3 bits of the address DAD3, 4, and 5, are decoded into eight

signals representing the eight possible states of the three bits, these eight signals are named 000 through 007. The next least significant 3 bits, DAD6, 7, and 8, are decoded into eight more signals representing the eight possible states of those 3 bits, called 00 through 07. The most significant 2 bits of the address, DAD9 and 10, are decoded into four signals, 0 through 3, representing the four possible states of those 2 bits. With this decoding of the Display Address signals, it is possible to describe any position in a sweep to a resolution of 8 bits, or one part in 256, by the use of a three input gate.

For instance, the marking of the position in the character groups where the characters start and end for the Main Time Base is done by setting a flip-flop TBA at 12B, output pins 5 and 6. The J input, pin 3, is driven by a three input negative input "and" gate output 12C08. The input terms 0, 00, and 007 describe an octal address, 007, where the flip-flop will be set. The K input, pin 2, is driven by a similar gate, 12C12, whose input signals are 0, 05, and 003. This set of terms describes an octal address, 053, where the Main Time Base characters end. Examination of the J and K gating terms for setting the flip-flops that mark the times of the various character groups reveals that Alternate Time Base (TBB at inputs 12B11 and 12) starts at 063 and ends at 127, Display Expansion Factor (Xpand at inputs 13B03 and 02) starts at 137 and ends at 207, Cursor Delta (Sample Intervals between cursors, at inputs 13B11 and 12) starts at 217 and ends at 277, and Vertical Voltage (Vertical Voltage difference between cursors when Analog plug-in module is used, at inputs 11B11 and 12) starts at 307 and ends at 363. The sweep ends and flyback starts after 377.

Two more functions are accomplished on this PC board having to do with the character display. These are the generation of Dot Count signals and Character Count signals to be used for the control and timing of character dot modulation of the Z axis input to the Display Unit. The binary Dot Counter at 13A starts counting character dots from zero at the beginning of each character group. Each character is allocated eight dots, even though these are only five dot columns in each character. For the character display, the first dot (or column) is settling time, the next five columns allocated to the five dot columns of each character and the last two columns are part of the three column space between this character and the next. The gate, output pin 14C06, feeds the count of column 7 to the binary Character Counter at 14A10, enable input, making it possible to count the characters within a character group. There is one short character, the period, which is cut short after four columns, to create a more favorable character spacing when the period is used. A signal from the Character Generator PC Board, Ch Negative Period, is used at 13A09 to cause the Dot Counter to be reset after the fourth column, and it is also used

through the gate at 14B09 to cause a "carry enable" to the Character Counter at 14A10. The details of this function will be covered in the section on the Character Generator.

The other circuits on the Display Control PC Board, on sheet 1 of the schematic diagram, deal primarily with the vertical and Z axis controls. The upper left corner of the diagram shows an eight input multiplexer circuit at 3A that is used to select the data from the Channel Memory outputs, one at a time. The circuit is addressed by the least significant three bits of the Sweep Address counter, at pins 3A09, 10, and 11. The memory addresses are cycled 16 times (once for each sweep) during each display cycle. The recall rate is 100 times slower than the fastest record rate, so power dissipation with the memory circuits caused by cycling during display is negligible. Also, it is a diagnostic aid to have the memory run continuously during Display Mode when trouble-shooting memory problems inside the instrument.

The serial data from the gate output at 4A08 is the correct channel gated with Sweep Address 4, Displot Mode, not Flyback, and another term formed by the flip-flop at 6D05 that interrupts the data stream when Last Memory Address occurs before flyback does. This can occur at any value of display expansion with the left cursor closer to the Last Memory Address location than the expansion factor allows in Sample Intervals in the display. For example, if the expansion is X2 and the left cursor is less than 50% of the Memory Addresses from the Last Memory Address, or if the expansion is X5 and the left cursor is less than 20% of the Memory Addresses from the Last Memory Address and so on for each expansion factor, the trace becomes blank when Last Memory Address is reached.

The flip-flop at 6D, output pin 08, with the gate 3E03 form an edge detector circuit that marks the first sweep dot after flyback. This signal is gated with Display Expand in the gate 4F11 to mark the left cursor when the display is expanded. The operation of the cursors is manual, individual, and independent except that the left cursor cannot be moved left of the left edge of the display, the right cursor cannot be moved right beyond the Last Memory Address, the right cursor cannot cross to the left of the left cursor, and when the display is expanded, the display is justified to the left cursor as a means of positioning the display at the desired portion of data to be inspected with large values of expansion. This signal, first dot in expanded display, is negative "or" gated at 4F10 with a composite left or right cursor signal from the gates 4B12, 4B10, 4C08, and 4C11 that is input to 4F09, and the signal at 4F08 might be called "any cursor start."

The flip-flops at 3D and 3F are connected serially, as a shift register, and serve to stretch each cursor marker by three display dots to make them more visible at low values of expansion. The first flop is asynchronously set by the "any cursor start" signal at 3D04, and is then clocked off by the display clock pulse

gated with the data advance signal through the gate at 3C11. The output 3D05 will be high to mark the cursor for the full width of the data bit being marked. In addition, the three remaining flip-flops are clocked by the sweep clock, so the last output, 3F06, will go high three sweep dots later, and through the gate 3E11 will stretch the cursor by that amount. The gate output 3E11 is used through R34 to make a small negative current charge to the summing node of the Vertical Deflection D/A converter, whose summing operational amplifier is at 1C-A. This cursor deflection, as seen in the display, is negative, or low, approximately 1/4 the vertical difference between logic 0 and logic 1 in the displayed data stream.

Another group of circuits using the gates at 3C03, 3C06, 3C08, 4D06, 4A06, and the flip-flops at 3B form a marker for the beginning of data cell for values of display expansion of 10 and greater. The terms Not Flyback, Sweep Address 4, Displot Mode, and Display Expand 10, 20, 50, 100, are gated together by the time they reach 4D06. Then they are gated with Display Data Advance at 3C03 and again with Sweep Positive Clock Pulse and inverted at 3C08 for use as the clock input to the first flip-flop at 3B03. Consider the case of expand X10. Both flip-flops start reset, with 3B06 and 3B08 high. The signal Display Data Advance is synchronous with the last display dot of each data cell for any value of expansion, making it the tenth dot for X10, and 3C08 gates through the last sweep clock pulse to clock 3B06 low. This in turn through gate 4A06 into 3C05 causes 3C06 and 3C09 to stay enabled until the cycle is complete. The two flip-flops are connected as a two-stage binary ripple counter, and the gate output 4A06 will stay low until the counters reach zero count when it will go high and disable the gate input 3C09. As long as the gate output 4A06 is low, the inverter 2E12 will furnish a position current charge through R35 to the summing node of the Vertical Deflection D/A Converter. The result in the display is a narrow positive spike at the beginning of each data cell during expansion values of X10 and more. This is useful in long strings of data of one polarity, making it possible to locate any single data cell by count without having to rely on transitions.

The group of two input multiplexer circuits at 2B and 2C are used to select the correct inputs for the Vertical Deflection D/A converter. The signal on pin 1 of both circuits with complete nomenclature would be called Digital Plug-In/Analog Plug-In, high for digital and low for analog. When pin 1 is high, input pins 3, 6, 10, and 13 are selected as inputs, and when pin 1 is low, input pins 2, 5, 11, and 14 are selected as inputs. During the first eight sweeps, either analog or digital, the character display is being produced by the Z-axis modulation of the raster produced by Sweep Addresses 1, 2, and 3 driving through the multiplexer at 2C to the least significant 3 bits of the Vertical Deflection D/A converter. Pin 2C01 may only be

driven low by 4C03 when Sweep Address 4 and Analog Plug-in signals occur together. The circuits at 2B are disabled by Negative Sweep Address 4 at pin 15 during the character display, and then enabled during the data sweep or sweeps. When an analog plug-in is used, the character display is followed by only one data sweep, which is the D/A conversion of the successive words represented by the contents of memory.

With a digital plug-in, the character display is followed by a raster of eight sweeps, with base lines located approximately on each of the eight graticule lines on the display, each sweep, from top to bottom, displaying the sequential data from the memory channels 1 through 8. The base lines represent data "zero" and the data "ones" are represented by positive vertical displacement of the base line approximately 4/10 of a major graticule, to create a swept display similar to that when measuring a repetitive logic time sequential signal with a triggered oscilloscope. The serial digital data is applied directly to the output attenuators from the output vertical amplifiers through the trimmer R62 and the series resistors R162 and R163. The data is applied in this fashion because the rise time requirements of the data exceed the bandwidth capability of the analog amplifiers at 1CA, 1C-B01, and 1C-B07.

The Vertical Deflection D/A converter is identical in nature to the one used for the Horizontal deflection, except that the Vertical D/A converter has only 8 bits. The most significant two are adjustable, instead of 11 bits with 5 adjustable. The operational amplifier buffers at 1C-B01 and 1C-B07 are connected as unity gain inverting amplifiers to satisfy the voltage polarity requirements of the display unit. Transistors Q1 and Q2 are connected identically to, and serve the same function for, Plot Y output as Q22 and Q23 do for the Plot X output. One significant difference in the Vertical Deflection signals is the use of the BCD to 10-line converter at 6B that is driven by the Sweep Address signals such that the outputs 6B01 through 6B07 and 6B09 are sequentially selected low for the data sweeps for Channel 1 through Channel 8.

The buffer follower operational amplifier at 6E-A07 is normally biased at approximately +4 V by the resistor series divider R173 and R174. This voltage is high enough to keep the diode CR50 back biased from the voltage at the top point of the divider string R172 and R33, which is slightly less than +4 V. The purpose of the switches, S1, located at circuit location 7F on the Display Control PC Board, is to deselect any channel display for the purpose of adding clarity to the display. For illustration, assume we wish to remove Channel 8 from the display, and we turn on the Channel 8 switch, which is one of eight miniature rocker switches mounted in a single dual-in-line plastic package. When the Sweep Address signals reach the combination selecting data sweep for Channel 8, 6B09 goes low, driving CR58 on, pulling 6E-A05 down to about +1 V. Pin 6E-A07 then pulls down R172 through the diode CR50, taking most

of the current out of R33. This, in turn, causes the D/A converter output 1C-A06 to go positive to compensate, causing the Display Vertical driver amplifiers at 1C-B01 and 1C-B07 go to equally negative and placing the Channel 8 sweep several volts below that required to keep it in the display. In this fashion, any of the eight digital data sweeps may be eliminated temporarily from the display.

The Z axis display output is driven by a modified D/A converter at 5AA, output pin 6, through a 2:1 resistive voltage attenuator R7 and R8 for the internal display unit, and through noninverting and inverting unity gain amplifiers for the External Z and External $\overline{Z}$ outputs for external use. A bias network, made up of R13, CR4, and CR3 provide a reference voltage for the input 5A-A03, which is at or near the switching threshold for TTL signals. The summing node inputs to 5A-A02 are diode-steered negative current sources, one for applying the character display data and the other for applying a steady signal during the time the data is to be displayed. Both current sources are individually trimmable, the data intensity by R64 and the character intensity by R63. The gate inputs 4E12 and 13 are driven by the gating of terms (Sweep Address 4, Not Flyback, Displot Mode, Not AD Last Memory), while the gate output 4E11 goes negative for increased intensity. This back biases CR14, allowing R63 and R37 to take current from the summing node, causing 5A-A06 to go positive to compensate, and causing an increase in Z-Axis intensity for data display. The same features of operation apply to the character signal input except that the Character Generator output is gated at 4E04 with Negative Sweep Address 4, Displot Mode on 4E05, and the gate output 4E06 going negative for an increase in intensity for each of the character dots to be displayed.

Character Display Control

The generation of timing control for the character display has already been described in the section covering the Display Control PC Board, where those timing signals are generated. However, a description of the mechanics of the character display will help in understanding the timing and character selection coding implemented in the 8200.

The characters are stored in a Read-Only Metal Gate MOS Memory circuit. The storage is permanent, not erasable by power turn on and off sequences, and not alterable from the external connections without damage to the circuit. The data is stored in the form of binary data bits, stored in an organized manner, that when recalled a seven horizontal row by five vertical column may be constructed of the outputs and the dot selection of the output "ones" will portray any of the ASCII Coded Characters. There are 64 characters, of which 26 are alphabet capitals, 10 are decimal numerals, and 28 are punctuation and algebraic symbols. Various manufacturers providing the circuits build them with slight variations in the character font created by the reconstructed

data bits, but any given character is addressable in any manufacturer's circuit by the same standardized ASCII code. One type will be described here and the differences of others pointed out.

Each character is addressable by the correct code on the six input address lines. There are also three Row Select control inputs to select the row of the character dots to be output on the five data outputs. The Row Select inputs are binary coded from top to bottom, code Ø selects a blank row above the character, making it possible to select "no output" from the circuit without having to drive a "chip enable" input. A binary 001 selects the top row of the character, on down to a binary seven (111), which selects the bottom row of the character. For each row selected, the dot data outputs will change depending on the font format of the character addressed. The circuit described here is the Signetics 2513N MOS-2560 Bit Static Read Only Memory.

The first sweep in the display cycle, Sweep Count Ø is used for cursor difference count arithmetic updating, and the next seven sweeps, Sweep Count 1 through Sweep Count 7, are character display sweeps. During Sweep Count 1, the sweep is carried from the left edge of the display straight through to the right edge, painting, or brightening, those character dots that have logic "1s" in the top row, progressing through the characters left to right, and through the dots of each character, left to right. After the flyback following Sweep Count 1, Sweep Count 2 progresses through the dots in sequence and characters in sequence, left to right, painting the dots in the second row from the top, and so on down through Sweep Count 7, for the bottom row of dots.

To repeat this operation and to consider how the signals occur at the Character Generator ROM circuit, starting at the left edge, or beginning of Sweep Count 1, remember that there are eight Sweep Clock Pulses, at 2 MHz per character dot, and there are 256 total possible dot locations across the sweep. Eight dot positions are reserved for the left margin, the next eight are for the first character of the first character group. At the beginning of the ninth dot, the six address inputs to 15B, pins 17 through 22, select the correct character. The row select lines are at row 1 where they will be for the entire sweep, and the character generator will output the signals representing the five dots in the upper row of the first character. These signals will be multiplexed through the 8-line to 1-line multiplexer at 14A, and its output for the zero for the first dot in the character is left margin. As the Dot Select lines are counted up, each of the dots of data will be output, ones or zeros, for counts 1 through 5, and then zero for counts 6 and 7, which are right margin for that character.

The Character Counter is then incremented, the new character selection is made at the address inputs to 15B, and the Dot Select lines count 0 through 7 for the first row dots of the second character, and so on through the first row dots of all the characters in the character display.

During the Flyback from Sweep Count 1, the Sweep Address lines are incremented, the Row Select lines are at row 2, and through Sweep Count 2 the same exact character address and character group selection as Sweep Count 1 is repeated, and the row 2 dots are pointed immediately below the row 1 dots. This same procedure is repeated for each sweep through Sweep Count 7, at the bottom of the character display.

The first two character groups to be displayed are the Main Time Base (TBA) and Alternate Time Base (TBB, left blank when in Single Time Base Mode). The Time Base control signals from the Control Register are the same ones used to control Time Base selection and are the same exact code as read from the Time Base selection lever switches. A group of two input multiplexer circuits at 11A and 12A determine which Time Base signals will be encoded to ASCII 6-bit character codes for addressing the character generator circuit. The outputs of the multiplexer circuits are used to drive two BCD to 10-line converters at 11B and 12B. The outputs of 11B are one line each for the "decade" selection of 0.1, 0.2, 0.5, 1, 2, 5, 10, 20, and 50, while the outputs 12B are one line each for the "seconds" selection of nsec, μsec, msec, and sec.

The combination gating that follows these signals is determined by inspection of the ASCII codes for those characters to be displayed for Time Base selection, namely 1, 2, 5, Ø, M, N, U, S, and period. The fact that the period is shortened from eight columns to four columns is of no concern here, as that timing correction is all accomplished on the Display Control Board. So the period is merely treated as a full character for character addressing. The four-line to one-line multiplexer circuits at 13D, 14D, and 15D sequence through the first four character times of each of the Main and Alternate Time Base groups, being addressed at pins 14 and 2 by the Timed Character Count lines from the Display Control Board. The fifth character time in each of the TBA and TBB groups is always an S. At this time the multiplexers for the first four character times are deselected at pins 1 and 15 on each of those circuits, and the "fifth character time" signal from 15F05 is active low, 13F02 is high, enabling the gates 11F03 and 08, which "or" gates the ASCII code for S (110011) through the gates 13E03, 11, 06, and 08.

Finally, these signals, which are the character address signals for TBA and TBB, are multiplexed with the other character group signals in four-line to one-line circuits at 13C,

14C, and 15C. The character group select signals that address these multiplexers lump the first two groups together, TBA and TBB, and TBXpand the second group selection, TB Delata (cursors) the third, with TBVertical Voltage the fourth group.

When the period character is sensed by the combination of gates at 12E, and the fourth column at 13A11, the gate output 13B06 signals the Display Control Board for shortening the dot count and advancing the character count. In addition, the character code being addressed to the character generator ROM is changed from a period to an underbar, the "the" gates at 13B03 and 13A08 control the character dot output to enable only the third and fourth dots to be fed to the Display Control Board. This character modification was required because of font differences between the character generator ROM circuits chosen as alternate devices for this application. Another modification required by this variation is the use of the gates at 16E08 and 15A11 to accept the inverted polarity dot outputs when the Fairchild 3258 DDC circuit is used. In addition, the Fairchild device has internal row count logic and requires a reset to Row Ø and a Row Advance signal for its operation. The gates at 13A03 and 13A06 and the gates at 13B08 and 13B11 create these signals from the Sweep Address and Row Advance signals from the Display Control Board.

. The seven BCD codes on three lines from the Display Expansion lever switch are converted to seven lines by the BCD to 10-line converter at 14F. There are five full characters in this group, TBX an X, a dash, and three decimal numerals. Again, simple inspection of the bits required by the character generator at the correct character times reveals the gating required for inputs to the four input multiplexer circuits at 14E and 15E. They are addressed by the gate outputs 16F06 and 16F03 to multiplex through character counts 1 through 4, ignoring character count Ø, during which time the character X is coded directly from 15F01, 15F02, 12C08, 14E09, and 15E07 and 09. The remaining characters are coded by the combinations from the gates at 13F and 16F, and multiplexed through the circuits at 14E and 15E for inputs to the character group multiplexer circuits at 13C, 14C, and 15C.

The cursor decimal difference characters are more easily coded because the BCD characters read from the counter already have the same identical code as the least significant 4 bits of the corresponding ASCII character. There are, however, six characters in this group, including the left and right arrow points, to identify the group visually. These two characters have the same bits coded as the numerals in the most significant 2 bits, so the coding for the entire group is accomplished by four circuits of eight input to one output multiplexers, addressed directly by the Character Count signals to sequence through first the left arrow point, then left to right through the four decimal numerals, and last the right

arrow point. These multiplexers are at 16A, 16B, 16C, and 16D. Their outputs drive the Delta group inputs to the character group multiplexers at 13C, 14C, and 15C.

The last character group, the Vertical Voltage group, is currently coded directly into the character group multiplexers as blank, or null, characters by hardwire means. At this writing, the analog plug-in has not been designed, and it is intended that those characters will be coded elsewhere in the instrument as that design dictates.

Cursor Display Control

The cursors are two separately movable markers for locating and marking any two sample interval events in a displayed recording. Each cursor is in the same position on each trace displayed. For example, if the left cursor is 200 sample intervals from the start of the record on Channel 1, then it is also 200 sample intervals from the start of the record on each of the other channels. The display will show them to be in a line, vertically above or below each other. The same position feature applies to the right cursor. The right cursor is always on or to the right of the left cursor, as they never cross over or exchange relative positions. The left cursor never moves left of Ø address, or the beginning of the record, and the right cursor never moves right of the Last Address, or end of record. The cursors are display features only, and so the controls for them are not reflected in the Control Register and are not remotely controllable, nor are they indicated in the data of any output, except for the display unit and the plot output.

Each cursor is position controlled by a spring-centered five-position (two positions either side of center) paddle switch, the pair mounted horizontally, directly below the Display Expand lever switch, just to the right of the Display Unit on the Main Frame Front Panel. The left switch is for the Left Cursor, and the right switch is for the Right Cursor.

When a cursor switch is moved nominally halfway to the right stop from center, that cursor moves at a slow rate to the right. When the switch is pushed to the right stop, the cursor moves at a fast rate to the right. When either cursor switch is moved half way to the left stop, slow cursor movement occurs while pushing either switch to the left stop causes the cursor to move to the left at a fast rate. If such motion causes either cursor to run into the other, or to run into the beginning or end of the record, the motion merely stops, regardless of switch position.

The schematic diagram for the Cursor Control Board shows the way in which these controls are affected. Two serially connected 4-bit binary synchronous counters, at 12F and 13F, are clocked by the 2-kHz clock pulse and provide two synchronized clock pulse rates for the cursor motion. The fastest rate, from 12F12, is 250 Hz, and with this clock pulse either cursor may be moved from one end of the record to the other in just over 8 sec. The slowest rate is slightly under 8 Hz, making it possible to stop cursor motion at nearly any predetermined spot on the display, or any predetermined difference count on the display by the cursor difference characters. The gate at 11F06 holds the counter disabled and "reset" anytime no cursor motion is required. When any motion, up or down, is requested, this gate enables the counter such that the first count is always a full count cycle, never slivered.

The cursor control switch contact arrangement is "break before make" for each contact set for one direction for each cursor. For example, to push either cursor switch halfway to the right stop "breaks" the first contact on that side. Pushing that switch to the right stop "makes" the second contact without disturbing the contact that was opened. The "arms" of all four contact sets are common to ground.

To consider the Left Cursor motion control, when the switch is in center position, 7A13 and 7A11 are at ground and 7A05 and 7A09 are high logic level. Two sets of cross-connected gates at 7C form two RS flip-flops for switch contact bounce elimination. When the Left Cursor switch is moved halfway to the right stop, the signal LC up slow goes high, 7A13 and 7C13 go high, 7C09 is forced low, and that flip-flop changes state with 7C08 going high and 7C11 going low. Pin 7D10 was already high, so the output 7D08 goes high enabling the and-or-invert gate input at 11B09. The clock pulse counter is also released at the same time, and after a minimum of 128 msec the first clock pulse trailing edge will appear at 11B10, inverted at 11B08. If the right cursor is right of the left cursor, 11C10 will also be low, and the clock pulse will be gated through 11C08 to the "up count" clock pulse input pin 12A05, incrementing that counter. This left cursor position counter at 12A, 13A, and 14A is a serially connected ripple up-down counter with separate up and down clock pulse inputs. The counter is never parallel loaded and is cleared to zero at power turn-on. The slow rate up clock pulses will continue to count the left cursor counter up until the switch is released or pushed to the right stop, or the left cursor runs into the right cursor. If the switch is pushed on to the right stop, the signal LC Up Slow stays high, and the signal LC Up Fast goes low, 7A06 goes high, 7D08 and 11B09 go low and the 250-Hz clock pulses at 11B13 are gated through, inverted at 11B08 and 11C09. If the right cursor is still right of the left cursor, the negative high speed up clock pulses will up-count the left cursor counter.

The controls for the left cursor down-count are identical to the up-count controls. The RS flip-flop at 7C03 and 7C06 eliminates the switch bounce and enables the gate input 7D12, which enables 11B04 to gate the slow clock pulse through to the left cursor counter down-count clock input. When the switch is pushed to the left stop, the signal LC Down Fast goes low, 7D13 and 11B04 go low, 11B03 goes high, and the high-speed clock pulses are gated through to the down-count input. The control input to the gate at 11C13 enables the left cursor to be counted down anytime except when the left cursor is at the left edge of the record, or zero, address.

The right cursor controls are duplicates of the left cursor controls. They are implemented with the inverters 7A02, 7A04, 6A12, 6A10, the two sets of cross-connected gates at 11E06, 11E03, 11E08, and 11E11 forming the RS flip-flops, and gates 7D03, 7D06, as well as and-or-invert gates at 11D08 and 11D06. The gate at 11C06 clocks the right cursor up-count clock pulses when the right cursor is at the right edge of the record, and the gate at 11C03 blocks the right cursor down-count when the right cursor count is not greater than the left. The right cursor counter is the series connected ripple up-down counter identical to the left cursor counter.

The right cursor "overflow" and the left cursor "underflow" signals are essentially "after the fact" signals, not suitable for inhibiting clock pulse gating. So the right cursor up-limit gating is accomplished with the 12 input nand gate at 14F, and the left cursor down-limit gating is accomplished by the gates at 11A12, 11A06, 11A08, 15A08, 7B11, 7B06, and 7B08. The "right greater than left" comparison is done with the series connected magnitude comparators at 12C, 13C, and 14C, and the "right greater than left" signal, through the inverter at 7E08, enables the left-up count and the right-down count.

The series connected magnitude comparators at 12B, 13B, and 14B are used to compare the Left Cursor address to the Display Address, comparing for equal. The signal at 14B06 provides a Left Cursor Sync signal to be used on the Display Control Board to mark the Left Cursor on the display when it is not expanded, and is also used for Cursor arithmetic as will be explained here. The Display Address is also compared to the Right Cursor address in the series connected magnitude comparators at 12D, 13D, and 14D, and the compare equal signal at 14D06 is used solely for the cursor arithmetic logic, as will be explained.

The counting and addressing of cursors and display sweep has all been done to this point in binary. The cursor difference count must be converted to BCD code for the character display, so a simple count conversion is made here in the following manner. The gate input pins at 11F09, 10, and 13 accept the signals Left Cursor Sync, Negative Right Cursor Sync, Sweep Count Ø, inverted at the output 11F05 to drive the cross-coupled gates at 7F03 and 7F06, forming an RØ RS flip-flop, to set it. The Right Cursor Sync inverted at 7E04 resets it at 7F05. The four decade synchronous BCD counter at 15F, 15E, 15C, and 15B is clocked by the Read Negative Clock Pulse, which is 2 MHz for Display Mode during the first eight sweeps. This counter is cleared to zero at pin 1 on each circuit by the gated signals Sweep Count Ø and Dot Ø, inverted at 7F08.

The display expansion does not pertain to the first eight sweeps, so, after being cleared, the counter is waiting, not enabled, for the Left Cursor Sync, which sets the flip-flop high at 7F03, enabling the counter. The Right Cursor Sync resets the flip-flop at 7F03, and the counter is disabled until the next Sweep Count Ø, so the difference count data is held in decimal, or BCD, code through the entire display of characters and data. The parallel outputs of the four decimal digits of the controls of this register are output off the board for use by the Character Generator Board. During the last eight sweeps (data sweeps) of the Display cycle, the Read Negative Clock Pulse is the Sweep Clock Pulse reduced in rate by the display expansion factor.

A second counter called the Decimal Down Counter at 16F, 16E, 16C, and 16B is a serially connected BCD ripple-down counter. A group of gates at 6A08, 16A11, 16A03, and 16A06 gate together the signals required to cause the Decimal Down Counter to be parallel loaded with the contents of the Decimal Difference Counter by the Left Cursor Sync of each data sweep when not expanded, and by Load Cursor Address at the beginning of each data sweep when expanded. This Decimal Down Counter is then counted down by the Read Negative Clock Pulse until it reaches zero count. The group of gates at 15A12, 15A06, 16D08, 15D11, 16D06, 16D12, 15D03, 15D06, and 15D08 decode the zero count and provide an output with a pulse as wide as a read count cycle, this pulse being the Right Cursor Sync used by the Display Control Board for the display.

Remote Input/Output and Interface

The schematic diagram for the Remote Input/Output PC Board shows the eight input to one output multiplexer circuits (16 of them) that make it possible for the instrument to output any selected 8-bit word of data from the Control Register (or the mode control status word) or the contents of memory one word at a time. Sheet 1 of the schematic diagram shows the multiplfexers at 1B, 1C, 2B, 2C, 5B, 5C, 6B, and 6C, and also shows the output gating that provides the required signals to the Remote Input/Output interface. The "or" gates at 2E and 2F gate through the eight signals from the eight multiplexer circuits on this sheet, or the eight signals from the eight multiplexer circuits on the other half of the board called RI-D010 through RI-D017, shown on sheet 2.

These two sets of signals are mutually exclusive, only one group of eight multiplexers being enabled at one time. The eight outputs of these gates are input to eight exclusive "or" gates at 2D and 3F the other input to each gate being used for polarity selection. If the control input is low, the gate is noninverting, and if the control input is high,

the gate is inverting. The outputs of these eight gates are input to the eight data inputs to the tri-state line driver circuits at 3D and 3E, which drive the data output signal lines to the remote device connected to the interface. The control input to each of these gates is driven by a signal, Output Enable, which causes the driver outputs to be open circuit when not enabled and to drive actively the line either positive or negative, depending on the polarity of the data being transmitted when enabled.

The eight multiplexer circuits on sheet 1 of the schematic diagram serve to select the correct register word representing front panel switch settings on the plug-in module, which the eight multiplexer circuits on sheet 2 serve to select the correct register word representing main frame front panel switch settings. In addition, those multiplexer circuits on sheet 1 also serve to select the memory output when it is being digitally output and to select the status word. The address lines of these 16 multiplexer circuits are driven indirectly by the Op-Code bits of the Remote Input lines. For a complete definition of the Remote Input/Output signals and Op-Code to Data and Control Register correspondence, refer to Section V of this manual. Basically, the least significant 4 bits of the Op-Code address the multiplexers. On this board these signals are RP Data Input 8 through 11 and are buffered, and polarity selected, by the "exclusive-or" gates at 14B called the Buffer Select 1, 2, 4, and 8. Buffer Select 8 is also inverted, at 14D08, for use by those multiplexers on sheet 1. The signals Buffer Select 8 and Buffer Select N 8 are used at the "circuit enable" inputs to the multiplexers, at pin 7, making the selection of either group of eight circuits mutually exclusive of the other eight. Because of the fan-out loading on each of these Buffer Select signals, they are buffered a second time in the noninverting gate circuits at 4D06, 4D08, 4D11, and 5D4 for use by the address inputs to the multiplexer circuits on sheet 1 of the schematic diagram.

The rest of the Remote Input signal lines are buffered by "exclusive-or" gate circuits, making it possible to select the polarity that may be required by a given remote device. There are seven small rocker switches mounted in a dual in-line package located at 14F, with one switch dedicated to selecting Command polarity, three for selecting the polarity of each of the three device Address bits, one for selecting polarity of the 13 Data Input signals including Op-Code, one for selecting polarity of the Flag output signal, and one for selecting polarity of the eight Data Output signals.

The Panel Multiplex Address counter is located on this board at 5F. The 2-kHz clock pulse from the Time Base PC Board is counted down by the flip-flop at 13F05 to a 1-kHz clock pulse for use by the PMAD counter. This clock pulse is free running after power turn-on, and the counter is hardwired enabled and so continues to count as long as power is on. The 1-kHz clock pulse is buffered for use elsewhere in the instrument by the gates at 16D08 and 16D11, and the four PMAD counter outputs are inverted and buffered by the inverters at 6F04, 06, 10, and 12 and the power gates at 4F.

The two Internal/External Control switches on the main frame front panel are gated together on this board by the gates at 1E03 and 1E11. To change the control mode from Internal to External or from External to Internal, both switches must be energized simultaneously in the same direction. This feature was included to help prevent the casually inquisitive individual from destroying data recorded after a painstaking setup by merely poking a single switch. The signals are grounded for active from these switches, and the two negative input "and" gates at 1E03 and 1E11 perform this logic function. The negative "or" gate at 1D03 allows the Negative Power Clear signal to ensure the instrument to be in Front Panel control at power turn-on. The RS flip-flops formed by the cross-connected gates at 1F03 and 1F11 latch the control mode data, and the clocked flip-flop at 4E06 synchronizes the change of state of the RS flip-flop to the 1-kHz clock pulse to prevent data slivering to the Control Register when changing from Internal to External control.

The three input Device Address bits, after being polarity selected by the gates at 14E08, 11, and 06, are gated together in the gate at 13E08, inverted at 14D10, and gated with a signal that is high when data output is requested in the gate at 12D06. This signal, buffered at 12D08 for fan-out, is the Output Enable signal. Thus, when the instrument is addressed and data output requested, the output line drivers are enabled and held enabled until the address changes or the input Op-Code, bit 5, changes state, indicating a change to data input mode.

The Command input signal is buffered by two series connected Schmitt Trigger inverter circuits at 14D02 and 14D12, polarity selected at 14E03, and used as the clock pulse input to a flip-flop at 13F11, which is enabled at 13F12 by the negative device address signal. The buffered and polarized Command signal is also gated at 12D01 with the decoded device address signal 12D02 to form a signal for enabling the Flag output driver at 14D10. The Internal Command flip-flop output pin 13F08 drives a pair of one-shot circuits connected

serially. The first one-shot produces a 50-nsec wide pulse starting at the leading edge of Internal Command (from 13F08). The second one-shot produces a 100-nsec wide pulse that starts at the trailing edge of the first pulse. The two complementary outputs of this second one-shot at 15F13 and 13F04 are called TCMD (Timed Command) and Neg TCMD. The signal TCMD, gated with External Program, and Data Input, inverted at 15D06, become a negative clock pulse for entering data into the Control Register via External Program Control. The 1-kHz clock pulse gated with Internal Program Control and inverted at 15D12 becomes the negative clock pulse for entering data into the Control Register when the instrument is under front panel control. These two clock pulse signals are mutually exclusive and are negative "or" gated at 12D output pin 11 for use by the Control Register.

7.29 Power Supply

The 8200 power supply is a switching-type supply to reduce both weight and power consumption. The unit is contained in its own chassis, which can be removed from the 8200.

The power supply consists of a chassis containing the converter printed circuit board and a cover, upon which is mounted the regulator board and the interconnection hardware. AC power enters via a 3-wire connector from the 8200 back panel; DC power is distributed to the instrument via a printed circuit board connector mounted on the side of the power supply chassis.

7.291 General Theory of Operation

Refer to block diagram, Figure 7.17. Power entering through the AC connector is rectified and filtered. The resultant DC is stepped down via a conventional step-down switching regulator to approximately 100 VDC. This voltage supplies a DC-to-DC converter, both isolating the outputs from the power line and providing the four separated voltages required.

The +5 V output from the converter is sensed via another small DC-to-DC converter (again to provide line isolation) and used to regulate the output of the switching regulator.

The resolution of turns in the secondaries of the DC-to-DC power converter is not high enough to provide accurate +15 V, -15 V, and -5.2 V levels. The converter, therefore, supplies three voltages that are slightly higher than required, and they are dropped to the required level by three conventional pass regulators on the regulator board.

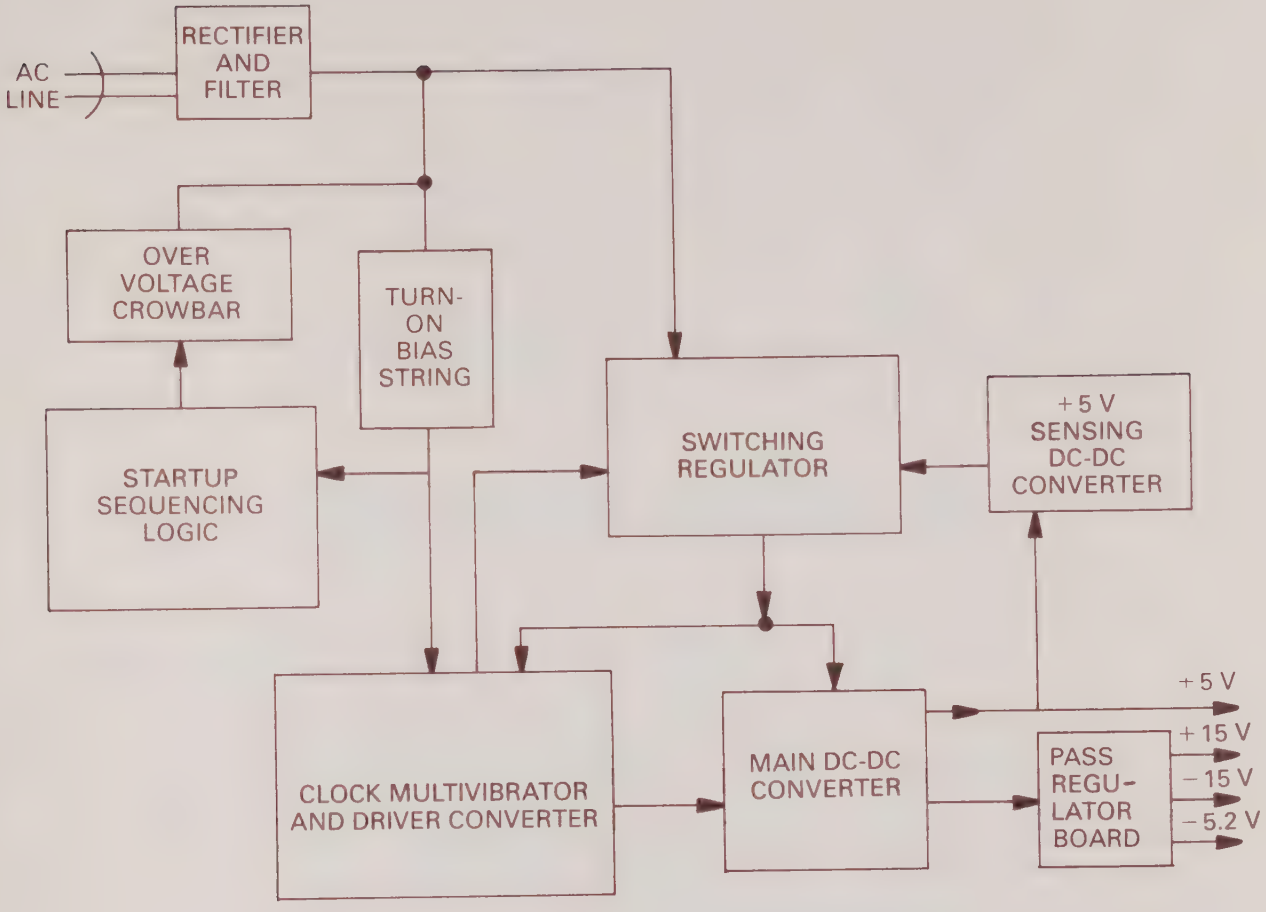


Figure 7.17 Power Supply Block Diagram

Timing signals for the switching regulator and the DC-to-DC converters are supplied by a multivibrator on the converter board. This multivibrator drives a third DC-to-DC converter on the converter board (called the clock converter), supplying isolated DC power to the switching regulator control circuitry and also base driving signals to the main DC-to-DC converter.

Additional circuitry on the converter board provides turn-on sequencing. To prevent large current surges from being drawn from the line when the 8200 is turned on, a resistor is inserted between the rectifier and its filter capacitors. The sequencing logic delays the turn-on of the converter until the capacitors are fully charged; once the converter is running, a relay shorts the resistor to avoid excessive power dissipation.

The output of the voltage comparator is applied through CR23 to a power driver (Q3-Q6) that supplies base drive to Q1, which in turn provides pulsating DC to the L-C filter.

CR23 and CR24 form an OR gate allowing Q1 to be turned off by either the voltage comparator, as described above, or by the current comparator (Q9-Q12). Current through L1 is sensed by the voltage across R33, which, after filtering, is applied to the base of Q11. If the voltage there exceeds the bias on the base of Q12, the comparator switches, turning Q1 off. Hysteresis in the comparator, generated by R55, assures that Q1 remains off until the current has reached a much lower value. Thus, the regulator is protected against short circuits. It should be noted, however, that the regulator is self oscillating in this current limit mode, and operates at 5 kHz or lower depending on the input voltage and degree of overload. This provides an audible notice of overload.

The main DC-to-DC converter consists of T3, Q30, and Q33. C30 and C31 provide turn-on delay in the base drive to prevent common conduction in Q30 and Q33. Q31 and Q32 act as current limiters to prevent excessive overcurrent spikes in case of overload. All output rectifiers are of the full-wave, center-tapped variety to reduce power dissipation.

Q22-Q27 and associated circuitry make up the clock multivibrator. Q22 and Q23 form a basic cross-coupled multivibrator, with Q24 and Q27 providing pull-up output drive current. Q25 and Q26 are part of a control loop that assure a 50% duty cycle in spite of capacitor tolerance. This is required to prevent biasing the transformer cores of the DC-to-DC converters. CR48 and CR49 square the output waveform, while CR51 and CR52 assure starting.

The clock converter's basic components are T1, Q28, and Q29. Q36-Q39 prevent common conduction in Q28 and Q29. CR59 and CR60 allow the turn-on sequencing circuitry to hold the converter off.

U1 and U2 perform turn-on sequencing and crowbar functions. Using CR12 as a reference voltage, U2 (output pin 1) monitors the input voltage and changes state when the input voltage is at a sufficient level to safely operate the converter. This state change begins time-out of a one-shot multivibrator formed by U2 (output pin 7). This gives C35 and C36 time to fully charge through resistor R104. After about 0.5 sec, U2 pin 7 goes low, turning off Q2 and enabling the converter. U1 (output pin 1) determines if the unit is operating above 180 V and, if so, readjusts the threshold of U2 (output pin 1) so that if the unit is turned off and then on again rapidly, the one-shot delay still is triggered. This prevents line surges that might blow the fuse.

U1 (output pin 7) monitors the output voltage of the switching regulator and changes state upon overvoltage, turning off the converter via CR10 and firing triac CR7 via CR8 and C1. This puts 15 Ω across the power line, rapidly blowing the instrument fuse.

Q20 and Q21, R34, R35, and CR38 provide power to the clock and sequencing circuitry when the converter is not running. When the converter is in operation, it provides the current through CR54, pulling the line up and back-biasing CR53, which turns off Q20 and Q21.

This concludes the technical description of the power supply. However, it is important to remember the following.

NOTE: All circuitry on the input side of the main converter is connected to the AC power line. Always connect the unit to an isolation transformer before trouble-shooting.

SECTION VIII

MAINTENANCE

8.0 Introduction

This section covers maintenance for trouble-shooting and repair of the Model 8200. Trouble-shooting is performed with the aid of a diagnostic procedure for the front panel controls and functions.

A PC board exchange program has been set up with the factory for use by customers within the continental United States, and with regional service centers in foreign countries. In addition, waveform photographs have been included with the schematics to aid service personnel who wish to trouble-shoot to the component level. Additional assistance in a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 255-9500, TWX 910 338 0226.

In summary, there are three methods of service available:

1. Return the entire unit to the factory or service center for repair.

2. Trace the problem to the defective PC board and obtain a replacement board from the factory or service center.

3. Trouble-shoot the problem to the component level with the aid of the diagnostic procedure and schematics or with the aid of factory personnel.

The following test equipment will be required to conduct the trouble-shooting procedure:

1. A pulse generator or function generator capable of fast rise time (<1 nsec) variable width pulses or square waves over the frequency range of 0.10 Hz to 100 MHz and with a variable output of up to 10 V peak-to-peak into a 50-Ω load.

2. An oscilloscope: 2 channel DC to 200 MHz input bandwidth.

8.1 Initial Setup

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
Power on machine, allowing 10 minutes for warmup. Check settings. 1. 50 nsec Time Base Main. 2. Single Time Base. 3. Internal Time Base. 4. Normal Dig. 5. Delayed Trigger Record Mode. 6. Normal Trigger Mode.	
No Display.	Check voltages. Check display intensity. Check for Trig Ready light on. If Trig Ready light is not on, check address control test-points 01 through 8. Unit is in Record Mode. Trig Ready light is on. Check display control Vert, Horiz, and Z testpoints. (See Display Control schematic). Sync sweep Ø. Hit Trigger Manual to see if Trig Ready light comes back on.
No response to front panel controls.	Check PMAD lines on Remote I/O) board TPs. Check test-points A-E on both sides of control register board sync on TP A. See Control Register schematic. Check 1 kHz TP on Remote I/O.

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
No characters on display.	Check display control test-points TBA, TBB, (Dual Time Base), TBX, TBO. Sync Swp Ø. See Display Control schematic.
No data sweeps.	Check channel deleter switches for Norm position. Check Vert testpoint Sync Swp Ø. See Display Control board.

8.2 Operational Modes

8.21 Select single mode, delayed trigger.

Arm Ready light is on. Depress Manual Arm and Trig Ready light will come on.	
Trig Ready light is on. Depress manual trigger and unit will go into a record cycle. Arm Ready light will come on when unit has finished a complete record cycle.	
Single Trig light is on and either Normal or Auto light is on.	Check for operation of front panel controls. Mode control board problem.
Arm Ready light does not go out when manual arm is depressed.	Check control register board for manual arm latch. Mode control board problem.
Trig Ready light does not go out when manual trig is depressed.	Check control register board for manual trig latch. Mode control board problem.
Trig Ready light does not come on when manual arm is depressed. Arm Ready light goes out.	Unit has received an external trigger and is in record. Mode control board problem.
Trig Ready light goes out when manual trig depressed, but Arm Ready does not come on.	Unit is receiving an Ext Arm Command.
	Unit is in record. Check record testpoint on mode control. Check for "AD MADR of 'OFL' L" from address control to mode control. Display will blank in record.

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
8.22 Select Auto Mode, Delayed Trigger	
Unit will have Auto light on and Trigger light will be lit dimly, reflecting internal triggering.	
Auto light is on and other mode selection lights are on.	Check for front panel control operations.
Auto light is on, Trig Ready light is on, there is no triggering.	Mode control trig pulsar is not working.
	"TB 200 PCP" from time base to mode control is not present.
Auto light is on, Trig Ready light is off, there is no display.	Unit is in pretrigger mode. Check DTM TP on mode control.
	Unit is in record.
8.23 Select Normal Mode, Delayed Trigger	
Unit will have Normal light on and Trig Ready light will be on. No triggering.	
Normal light is on and other mode selection lights are on.	Check for front panel control operations.
Normal light is on, Trigger light is off, there is no display.	Unit is in pretrigger mode.
	Unit is in record.
Normal light is on, manual trigger is depressed, Trig Ready light stays on.	Check control register manual trigger latch.
	Mode control board problem.
8.24 Select Pretrigger Mode, Single Mode	
In pretrigger mode the arm function initiates record and trigger ends record. When in auto or normal mode arm is initiated internally as part of the machine cycle. Select pretrigger mode, depress single mode switch, zero trig delay.	

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
When arm is depressed, unit does not go into record. Arm Ready light goes out.	Check for front panel control operation. Check that DTM testpoint on mode control board is low. Check gate 15D-6 on mode control for entry in record on manual arm.
Unit is in record, Trig Ready light is on, manual trigger is depressed, unit stays in record, Trig light does out.	Check for front panel operation. Check that DTM testpoint is low on mode control.
	Mode control receives "TD N CNT" from trigger delay to set end then "stop" for synchronous exit from record. Check trigger delay board "TP TD NCNTØ." Check mode control "TP STOP" for high level.

8.25 Select Normal Mode, Pre-trigger

Unit will have Normal light on, Trig Ready light will be on, unit will then be in record and display will be blank. When manual trigger is depressed, unit will momentarily have a display then internal arm as part of the machine cycle will arm the unit back into record.

Normal light is on, Trig Ready light is off, Display is off.	Unit is receiving Ext Trigger. Unit is triggering. Mode control board.
Normal light is on, Trigger Ready light is off, Display is on.	Unit did not go into record with external arm. Mode control board problem.

8.3 Record Basic

Setup:

1. Auto Mode.

2. Delayed Trigger.

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
3. Threshold A, all eight channels.	
4. 50 Ω/GND imp all eight channels	
5. Threshold A to -2.00 V.	
6. Threshold B to +2.00 V.	
All eight channels will reflect all ones in their memories. Auto trigger will record this. Change Threshold A to +2.00 V; the eight data channels will not show all zeros in their memories.	
Channel does not record ones in memory.	Move Threshold B to -2.00. If data channel changes state (zeros to ones) then check threshold select switch for that channel. Check threshold settings at testpoint TH A for correct operation on mode control board. Check testpoint WRT on memory boards for positive going pulses. Check for sample clock on plug-in.
When Threshold A is changed to +2.00 V, any or all channels do not change to zeros in memory.	Repeat checks for "channel does not record ones in memory."
Change all threshold selects on plug-in to Threshold B and repeat Step 8.3.	Repeat checks for "channel does not record ones in memory."

8.4 Record Normal

Setup:

1. External Trigger to plus (+) slope.
2. Select all channels Threshold A.
3. Threshold A and B to 1.00 V.

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
4. Select Normal Mode.	
5. Select Internal Trigger Channel 1.	
6. All Combination Trigger Switches.	
To middle (Don't Care) position, input a square wave (approximately 5 msec) into Channel 1. Select Channel 1 combinational trigger to the "Ø" position. Unit should be triggering (Trig Ready light dim) and Channel 1 data should have a square wave on it. Change the combinational trigger of Channel 1 to the "1" position. The display data should reflect the change in triggering edge.	
Normal light is on, Trigger light is on.	Unit not triggering off of Int channel. Check combo trig switches. Check for Int Channel 1 switch in internal Channel 1 position. Check combinational trigger input to trigger delay board.
Nonsynchronous data in memory.	Combinational trigger not working properly on plug-in. Trigger output on trigger delay board to mode control is nonsynchronous.
No square wave in memory.	Swap memory board with another channel. Check memory address lines from address control board.
Place the trigger out on the pulse generator to the Ext trigger input on the front panel and select Ext trigger. Synchronous triggering may be checked exclusive of the combinational trigger.	
Repeat check for all eight channels and their respective combinational trigger settings.	

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
8.5 Trigger Delay	
Repeat the setup as in Record Normal, Section 8.4, with the exception of the input pulse being 5 µsec with an interval of 100 msec. Unit should have a consistent triggered display of data.	
As the trigger delay setting is increased the data will move across the screen from right to left by the number of sample intervals set in the trigger delay switches.	
No delay effect from settings.	Check for "MC Arm Event" to the trigger delay board. This pulse is used to load front panel delay count into the delay counters. Check for trigger delay data into control register latches. See Trigger Delay schematic.
For verification of calibration of time delay, measure the positive going pulse on testpoint "DLY ENB" on the trigger delay board. Verify to computation below:	
TB X Delay = POS TIME TP "DLY ENB."	
8.6 Arm Ext	
Setup:	
1. Set Threshold A to +1.00.	
2. Set Threshold B to -1.00.	
3. Select Single Mode.	
4. Select Arm Threshold A.	
Input a square wave greater than 1.0 V to the external arm input. Unit will arm and Trigger Ready light will come on. Depress manual trigger and Arm Ready light will come on momentarily as unit arms. The 8200 will then halt in trig ready state.	

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
Arm Ready light stays on. Manual arm works.	Unit did not arm. Check upper left pin of Lemo connector for proper threshold A selection and setting. Trigger delay board. Check arm testpoint.
Arm Ready light stays on. Manual arm does not work.	Check control register for manual arm latch. Mode control arm not functioning. Check trigger delay TP arm to verify Ext Arm working.
Arm Ready light goes out. Trigger Ready light not on.	Mode control problem.

8.61 Arm Polarity

Trigger the scope on the trig out signal from the pulse generator and view testpoint arm on the trigger delay board. The arm pulse will move from the positive edge to the negative edge of the trig out signal as arm polarity is changed from (+) to (-).

No change in pulse polarity.	Check control register for arm (+/-) latch operation. Trigger delay board problem.

8.7 Trigger Ext

Setup:

1. Normal Mode.
2. Threshold A to +1.00.
3. Threshold B to -1.00.
4. Select Threshold A.
5. Select Ext Trig.

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
Input a square wave into the Ext Trig input and unit will start triggering. Trig Ready light will be dim. Select Threshold B and unit will stop triggering. Trig Ready light on.	
Threshold A selected. Unit does not trigger.	Check for proper selection of Threshold A and settings. Check trigger delay TP trig for pulse. Mode control not accepting Ext Trig input. Check through control register and trigger delay for selection of "Ext Trig" not "Int Channel 1."
Selection of Threshold B does not stop triggering.	Check through control register and trigger delay selection and settings on Threshold B.
8.71 Trig Polarity	
Trigger the scope on the trig out signal from the pulse generator and view testpoint trig on the trigger delay board. The arm pulse will move from the positive edge to the negative edge of the trig out signal as the trigger polarity is changed from (+) to (-).	
No change in pulse polarity.	Check control register for trig (+/-) latch operation. Trigger delay board problem.
8.8 Time Base Main	
Place the scope probe on the time base main testpoint and verify with the scope time base settings from 0.1 µsec to 5 sec.	
No time base or incorrect settings.	Check 20 MHz from clock generator to time base pin S136. Check time base control register latch settings. Time base board problem. Check main/alt time base control register latch operation.

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
For settings of 5 nsec through 50 nsec view time base at U7C-5 on digital plug-in.	
No 5 nsec to 50 nsec time base.	Check control register latches for 5 nsec to 50 nsec setting. Check outputs of 14A on time base board for nanosecond range enables.
	Clock generator problem.
Time Base Alt. Select dual time base. Place the scope probe on time base alt testpoint. Verify settings from 0.1 µsec to 5 sec. Note: Alt Time Base is a limited duration signal.	
No Alt Time Base.	Check control register for Alt Time Base latches and for dual time base latch.
For settings on 5 nsec through 50 nsec view time base at U7C-5 on digital plug-in.	Time base board problem.
	Clock generator problem.
	Mode control problem.

8.9 Dual Time Base - Delayed

Setup:

1. Select Dual Time Base.
2. Main Time Base to 5 nsec.
3. Alt Time Base to 20 nsec.
4. Select Trigger Delay of 050.
5. Select Normal Trigger Mode, Int Channel 1 Trigger.
6. Select Channel 1 Combinational Trigger on Plug-in to the "1" Position. All others to middle or "Don't Care" positions.

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
7. Select Channel 1 to Threshold A. 8. Set Threshold A to +1.00 V. Input a 1-µsec square wave with a 1.5 V amplitude into Channel 1. The first 500 words of the display will show two to three pulses. The last 1500 words of display clocked at 20 nsec will display approximately 12 times as many pulses as the first 500 words. 3 (times display length) X 4 (times sample interval) = 12	
No change in time base at 500 word mark.	Check trigger delay operation. See trigger delay section. Verify dual time base through control register latch to mode control enable. Sync (+) on trigger delay board test point "delay enable." View mode control testpoint "TB ALT" for positive transition at the end on trig delay "delay enable." Check clock generator for Main/Alt time base switching. Verify alt time base switch settings through control register latches. See Time Base schematic.

8.91 Dual Time Base - Pretrigger

Setup:

1. Retain the same setup as in delayed. Verify that dual time base delayed works properly before switching to pretrigger.

2. Select pretrigger mode. The display will now show the 5 nsec time base for the first 1500 words. The last 500 words will reflect a 20 nsec time base.

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
No change in time base, all 5 nsec.	Check switching at mode control testpoint "DTM" to a low level when Pretrigger is selected. Sync (+) on trigger delay TP "Delay Enable" and verify that on the trailing edge of "Delay Enable" mode control testpoint "Rec" goes from a high logic level to a low one ending record. Testpoint "Stop" on mode control will also go high on trailing edge of "Delay Enable." See Time Base schematic.

8.10 Remote I/O Write

Setup:

1. Set the I/O Polarity switches to the GND position (toward the connector end of board).

2. Select Ext program.

3. Issue a write command. The testpoints A0 through A3 will reflect the condition of command word bits 8 through 11, respectively. The leading edge of command will trigger "NCPCR." View testpoint NCPCR for pulse. Positive going command pulse selected.

No "NCPCR" pulse at testpoint.	Check "Ext Program" testpoint for high level. Check for correct addressing of unit. I/O polarity switches at GND level gives unit address Ø. Check for proper operation of "CMD" polarity switch.
Incorrect command executed.	Verify function code at testpoints A0-A3 (bits 8-11). Verify proper polarity and operation of "DI" polarity switch.

DIAGNOSTIC PROCEDURE	TROUBLE-SHOOTING PROCEDURE
No "flag" return out of 8200.	On I/O board "$\overline{\text{TCMD}}$" sets and resets 5E for flag pulse. "CMD" and address compare at 12D-5, enabling the flag pulse out. Check proper operation of "FLG" polarity switch. See Remote I/O schematic.

8.101 Remote I/O Read

Setup:

1. All polarity switches to the GND position, toward the connector end of the board.

2. Select Ext program, depress both Ext program switches simultaneously. Verify that Ext Prog lights are on.

3. Issue a read command with command bits 12 and 11 low. The data read from the control register will be available at remote I/O testpoints 10 through 17.

4. Issue a read command with bit 11 high. Data will now be available at testpoints 0-7.

No data out from 8200.	Check operation of all polarity switches. View testpoint "OUT EN" for positive pulse triggered by CMD in. Check addressing of 8200. Verify function code (bits 8-11) at testpoints A0-A3, respectively. Verify Ext program selected at TP Ext Prog being high. Check input command word and "command" for correctly selected polarity.

8.11 External Program Diagnostic Procedure

If the 8200 is normally used with a digital computer or another digital control device, use the following diagnostic program for checking out and trouble shooting the remote function of the 8200. The program shows OC-5, the Read/Write bit, in a logic one position denoting a write command. To check the result of the write command a read command (OC-5 low) must follow the write command with a comparison on data bits D I/O-1 through D I/O-8.

Instruction #	Command Word													Op-Code
	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	1	1	1	1	1	0	1	1	1	0	0	0	0	STATUS
01	1	0	0	0	0	0	0	0	0	0	0	0	0	T/B MAIN
02	1	0	0	0	0	0	0	0	0	0	0	0	1	
03	1	0	0	0	0	0	0	0	0	0	0	1	0	
04	1	0	0	0	0	0	0	0	0	0	1	0	0	
05	1	0	0	0	0	0	0	0	0	1	0	0	0	
06	1	0	0	0	0	0	0	0	1	0	0	0	0	
07	1	0	0	0	0	0	0	1	0	0	0	0	0	
08	1	0	0	0	0	0	1	0	0	0	0	0	0	
09	1	0	0	0	0	1	0	0	0	0	0	0	0	
10	1	0	0	0	0	0	0	0	1	0	1	1	1	T/B MAIN
11	1	0	0	0	1	0	0	0	0	0	0	0	0	T/B ALT
12	1	0	0	0	1	0	0	0	0	0	0	0	1	
13	1	0	0	0	0	0	0	0	0	0	0	1	0	
14	1	0	0	0	0	0	0	0	0	0	1	0	0	
15	1	0	0	0	0	0	0	0	0	1	0	0	0	
16	1	0	0	0	0	0	0	0	1	0	0	0	0	
17	1	0	0	0	0	0	0	1	0	0	0	0	0	
18	1	0	0	0	0	0	1	0	0	0	0	0	0	
19	1	0	0	0	0	1	0	0	0	0	0	0	0	
20	1	0	0	0	1	0	0	0	1	0	1	1	0	T/B ALT
21	1	0	0	1	0	0	0	0	0	0	0	0	0	TRG DLY I
22	1	0	0	0	0	0	0	0	0	0	0	0	1	
23	1	0	0	0	0	0	0	0	0	0	0	1	0	
24	1	0	0	0	0	0	0	0	0	0	1	0	0	
25	1	0	0	0	0	0	0	0	0	1	0	0	0	
26	1	0	0	0	0	0	0	0	1	0	0	0	0	
27	1	0	0	0	0	0	0	1	0	0	0	0	0	
28	1	0	0	0	0	0	1	0	0	0	0	0	0	
29	1	0	0	0	0	1	0	0	0	0	0	0	0	
30	1	0	0	1	0	0	0	0	0	0	0	0	0	TRG DLY I
31	1	0	0	1	1	0	0	0	0	0	0	0	0	TRG DLY II

Instruction #	Command Word													Op-Code
	12	11	10	9	8	7	6	5	4	3	2	1	0	
32	1	0	0	1	1	0	0	0	0	0	0	0	1	TRG DLY II
33	1	0	0	1	1	0	0	0	0	0	0	1	0	
34	1	0	0	1	1	0	0	0	0	0	1	0	0	
35	1	0	0	1	1	0	0	0	0	1	0	0	0	
36	1	0	0	1	1	0	0	0	1	0	0	0	0	
37	1	0	0	1	1	0	0	0	0	0	0	0	0	
38	1	0	0	1	1	0	0	1	0	0	0	0	0	
39	1	0	0	1	1	0	1	0	0	0	0	0	0	
40	1	0	0	1	1	1	0	0	0	0	0	0	0	
41	1	0	0	1	1	0	0	0	0	0	0	1	1	TRG DLY II
42	1	0	1	0	0	0	0	0	0	0	0	0	0	ARM/TRG
43	1	0	1	0	0	0	0	0	0	0	0	0	1	
44	1	0	1	0	0	0	0	0	0	0	0	1	0	
45	1	0	1	0	0	0	0	0	0	0	1	0	0	
46	1	0	1	0	0	0	0	0	0	1	0	0	0	
47	1	0	1	0	0	0	0	1	0	0	0	0	0	
48	1	0	1	0	0	0	1	0	0	0	0	0	0	ARM/TRG
49	1	0	1	0	1	0	0	0	0	0	0	0	0	OUTPUT MODE
50	1	0	1	0	1	0	0	0	0	0	0	0	1	
51	1	0	1	0	1	0	0	0	0	0	0	1	0	
52	1	0	1	0	1	0	0	0	0	0	1	0	0	
53	1	0	1	0	1	0	0	0	0	1	0	0	0	
54	1	0	1	0	1	0	0	0	1	0	0	0	0	
55	1	0	1	0	1	0	0	1	0	0	0	0	0	
56	1	0	1	0	1	0	1	0	0	0	0	0	0	
57	1	0	1	0	1	1	0	0	0	0	0	0	0	
58	1	0	1	0	1	0	1	0	1	1	0	0	0	OUTPUT MODE
59	1	1	0	0	0	0	0	0	0	0	0	0	0	TH A/B CH 1-8
60	1	1	0	0	0	0	0	0	0	0	0	0	1	
61	1	1	0	0	0	0	0	0	0	0	0	1	0	
62	1	1	0	0	0	0	0	0	0	0	1	0	0	
63	1	1	0	0	0	0	0	0	0	1	0	0	0	TH A/B CH 1-8

Instruction #	Command Word													Op-Code
	12	11	10	9	8	7	6	5	4	3	2	1	0	
64	1	1	0	0	0	0	0	0	1	0	0	0	0	TH A/B CH 1-8
65	1	1	0	0	0	0	0	1	0	0	0	0	0	
66	1	1	0	0	0	0	1	0	0	0	0	0	0	
67	1	1	0	0	0	1	0	0	0	0	0	0	0	
68	1	1	0	0	0	1	1	1	1	1	1	1	1	TH A/B CH 1-8
69	1	1	0	0	1	0	0	0	0	0	0	0	0	TH A1 S/L
70	1	1	0	0	1	0	0	0	0	0	0	0	1	
71	1	1	0	0	1	0	0	0	0	0	0	1	0	
72	1	1	0	0	1	0	0	0	0	0	1	0	0	
73	1	1	0	0	1	0	0	0	0	1	0	0	0	
74	1	1	0	0	1	0	0	0	1	0	0	0	0	
75	1	1	0	0	1	0	0	1	0	0	0	0	0	
76	1	1	0	0	1	0	1	0	0	0	0	0	0	
77	1	1	0	0	1	1	0	0	0	0	0	0	0	
78	1	1	0	0	1	0	0	1	0	0	0	0	1	TH A1 S/L
79	1	1	0	1	0	0	0	0	0	0	0	0	0	TH B1 D/A
80	1	1	0	1	0	0	0	0	0	0	0	0	1	
81	1	1	0	1	0	0	0	0	0	0	0	1	0	
82	1	1	0	1	0	0	0	0	0	0	1	0	0	
83	1	1	0	1	0	0	0	0	0	1	0	0	0	
84	1	1	0	1	0	0	0	0	1	0	0	0	0	
85	1	1	0	1	0	0	0	1	0	0	0	0	0	
86	1	1	0	1	0	0	1	0	0	0	0	0	0	
87	1	1	0	1	0	1	0	0	0	0	0	0	0	
88	1	1	0	1	0	0	0	1	0	0	0	0	1	TH B1 D/A
89	1	1	0	1	1	0	0	0	0	0	0	0	0	TH A/B II
90	1	1	0	1	1	0	0	0	0	0	0	0	1	
91	1	1	0	1	1	0	0	0	0	0	0	1	0	
92	1	1	0	1	1	0	0	0	0	0	1	0	0	
93	1	1	0	1	1	0	0	0	0	1	0	0	0	
94	1	1	0	1	1	0	0	0	1	0	0	0	0	
95	1	1	0	1	1	0	0	0	0	0	0	0	0	TH A/B II

Instruction #	Command Word													Op-Code
	12	11	10	9	8	7	6	5	4	3	2	1	0	
96	1	1	0	1	1	0	1	0	0	0	0	0	0	TH A/B II
97	1	1	0	1	1	1	0	0	0	0	0	0	0	
98	1	1	0	1	1	0	0	0	0	0	0	0	0	TH A/B II
99	1	1	1	0	0	0	0	0	0	0	0	0	0	B9-B16
100	1	1	1	0	0	0	0	0	0	0	0	0	1	
101	1	1	1	0	0	0	0	0	0	0	0	1	0	
102	1	1	1	0	0	0	0	0	0	0	1	0	0	
103	1	1	1	0	0	0	0	0	0	1	0	0	0	
104	1	1	1	0	0	0	0	0	1	0	0	0	0	
105	1	1	1	0	0	0	0	1	0	0	0	0	0	
106	1	1	1	0	0	0	1	0	0	0	0	0	0	
107	1	1	1	0	0	1	0	0	0	0	0	0	0	B9-B16
108	1	1	1	0	1	0	0	0	0	0	0	0	0	B1-B8
109	1	1	1	0	1	0	0	0	0	0	0	0	1	
110	1	1	1	0	1	0	0	0	0	0	0	1	0	
111	1	1	1	0	1	0	0	0	0	0	1	0	0	
112	1	1	1	0	1	0	0	0	0	1	0	0	0	
113	1	1	1	0	1	0	0	0	1	0	0	0	0	
114	1	1	1	0	1	0	0	1	0	0	0	0	0	
115	1	1	1	0	1	0	1	0	0	0	0	0	0	B1-B8
116	1	1	1	1	1	1	1	0	1	0	0	0	0	STATUS
117														
118														
119														
120														

SECTION IX

SCHEMATICS AND ASSEMBLY DRAWINGS

9.0 Abstract

This section contains information on logic symbols and reference designators, power supply removal and installation, display removal and installation, memory mother board removal and installation, and power supply conversion 110/220. Also included are schematics, assembly drawings, and diagnostic and mechanical illustrations.

9.1 Introduction

To better use, and more fully understand, the schematics and other documentation pertaining to the 8200, some explanation of the method and theory of PC board name, location, connector pin name, organization, signal name, and test point name identification is in order. For example, a typical signal might be called "200-MHz Sample Interval Positive ECL Clock Pulse - Trigger Delay." Clearly, this identification does describe the signal and identifies the destination, which is useful when identical signals are used to satisfy fan-out requirements. Also, a schematic with each point so named would have little room left for the components and circuits (the schematic size would be large enough to be suitable for wallpapering or otherwise difficult to use).

In the other extreme, the same clock pulse signal might be simply given a number, like 982. Such identification clearly saves space on the schematic diagram, but it is relatively useless without the technique of memorization of perhaps a separate supporting document to provide the details about the signal. In the 8200, signal name abbreviations have been used as a compromise from the long signal name, and yet with enough information in the name that a supporting document is not needed. For example, CG BYTE CLK 6 is a signal originating on the Clock Generator board, it is a byte clock, and its destination is the Channel 6 memory board. For convention, the name of each signal leaving a PC board starts with a two or three letter abbreviation of that board name. The following is a list by name and abbreviation of the PC boards used in the 8200.

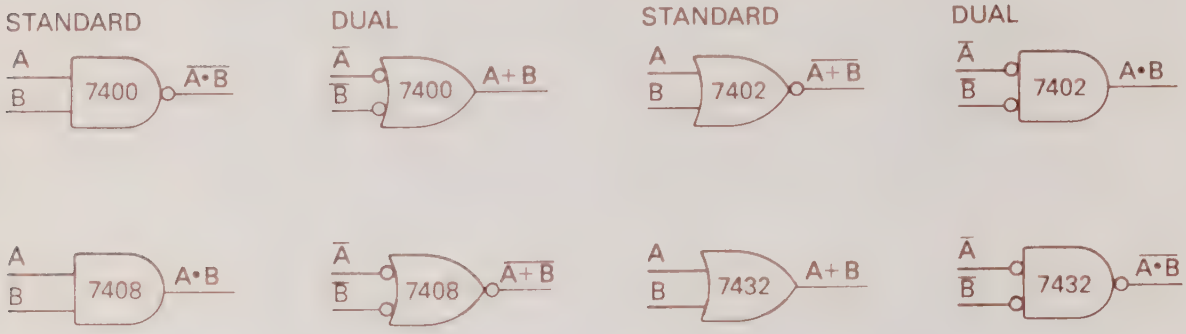
ABBREVIATION	NAME
PP	Plug-In Front Panel
TH	Threshold Selector
PI	Plug-In Logic Board
FP	Main Frame Front Panel
CG	Clock Generator
MEM	Channel Memory
DC	Display Control
CH	Character Generator
CU	Cursor Control
AD	Address Control
TB	Time Base
MC	Mode Control
TD	Trigger Delay
CR	Control Register
RIO	Remote Input/Output
RP	Rear Panel (Remote I/O Connector)

In addition to identifying the source and destination boards in the signal name, a negative level active signal is identified by an N following the source board abbreviated name. For example, DC N Swp Ad 4 is a signal originating on the Display Control Board and the signal is Negative Sweep Address 4. Names without N following the source initials are positive active. The original intent with regard to logic notation was that all negative active signals emanate from logic gate and device symbols with balloon outputs, such as positive input negative output nand gates. The convention used on clock pulses was that the trailing edge be the active edge, such that the positive going edge of negative clock pulses cause clocking action in flip-flops and counters. For devices using the negative going edge, the clock pulse is positive to maintain synchronized clocking operation throughout the instrument. Exceptions to this convention will be explained in Section 7.2 for that circuit.

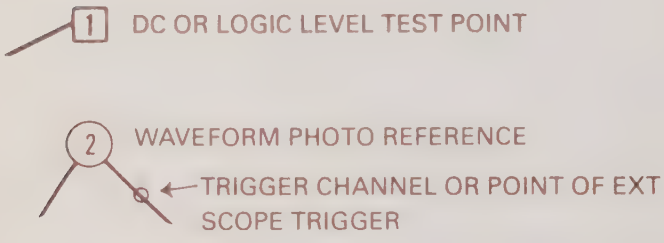
9.11 Logic Symbols

The Logic Symbols used in this manual depict the logic function performed and may be different than those published in the manufacturers' data books.

For example:



Reference Designators



9.12 Schematic Photographs

Some of the schematics in the latter part of Section IX have logic recorder photographs. Each photograph has a caption describing the function being shown. Because the machine is comprised of synchronous logic, there is a definite relationship in the sequence of events, varied only by the time base setting.

The events can easily be viewed on a dual channel scope because all of the events have a relationship synchronous with the trigger event. The trigger event is always the first displayed signal, reading top to bottom. The waveform recorder allows simultaneous viewing of all events, but is not necessary for viewing the depicted event. All events may be viewed by triggering on one channel and viewing the other events on the second channel when using a dual channel triggerable scope.

9.2 Power Supply Removal and Installation

9.21 Equipment needed: Crosshead screwdriver

1. Remove AC power cord from rear panel.

2. Remove both side covers and top cover.

3. Remove all logic boards from the power supply side of the 8200.

4. Disconnect the front panel on-off switch AC cable located at the bottom of the logic board section. See Figure 9.3, Steps 1 and 2.

5. Figure 9.1, Step 1.

   A. Remove the five protection plate retaining screws.

   B. Remove the power supply retaining screws.

6. Figure 9.1, Step 2.

   A. Remove the power supply protection plate as per the directional arrows.

7. Figure 9.2, Step 1.

   A. Remove the I/O connector retaining screws and the access cover retaining screws.

   B. Insert the access cover through the rear panel as per Figure 9.2, Step 2.

   C. Remove the rear panel perimeter screws.

      CAUTION: Prevent rear panel from falling after removing screws.

8. Figure 9.3, Step 1.

   A. Unplug the display unit AC cable and the power supply AC cable, and remove the rear panel from the machine.

      CAUTION: Make sure the I/O rear panel connector does not catch on the rear panel when removing.

9. Figure 9.3, Step 2.

   A. Remove the power supply from the 8200 through the rear of the machine as per the directional arrows.

9.22 Installation

1. To reinstall the 8200, reverse the order of events for removal.

   CAUTION: When reinstalling the rear panel, care must be taken to avoid pinching wiring to chassis. See Figure 9.4, Step 1 for caution points.

2. Check that the power supply AC cable is fed through its designated cut-out to avoid pinching to chassis. See Figure 9.3, Step 1.

3. Check from the top to ensure that the display power cord is not pinched between transformer shield and display unit.

4. When reinstalling logic boards, connect the front panel on-off switch AC cable first.

5. When installing the trigger delay board, check for proper installation of the co-ax cable to the board mounted connector. See Figure 9.8, Step 2.

9.3 Display Removal and Installation

9.31 Equipment needed: Crosshead screwdriver, no. 6 hex nut driver, and 0.050 Allen wrench.

1. Remove the power supply as per power supply removal section.

2. Remove the display unit retaining screws, Figure 9.4, Step 2.

3. Figure 9.5, Step 1.

   A. Remove the digital module plug-in from the front of the 8200.

   B. Remove the display control knobs with a 0.050 Allen wrench.

C. Remove the front panel retainer nuts with a No. 6 hex nut driver. The nuts are located on the rear of the front panel. The positions of each are noted.

D. Remove the front panel. At this point the only thing retaining the front panel is the connector located at lower center of the front.

9.32 Installation

1. To reinstall the display unit, reverse the order of events for removal.

9.4 Memory Mother Board Removal and Installation

9.41 Equipment needed: Crosshead screwdriver, flat edge screwdriver, and inspection mirror.

1. Remove the AC power cord from rear of machine.

2. Remove the memory boards and the clock generator boards.

   CAUTION: Remove the clock generator co-ax (Figure 9.6, Step 1) before removing clock generator board.

3. Remove the card guide retainer screws (Figure 9.6, Step 2) and remove the card guides.

4. Remove the rear panel access cover (Figure 9.6, Step 1) and disconnect the time base out interconnects (Figure 9.6, Step 4).

5. Remove the voltage transfer screws (Figure 9.6, Step 3).

   CAUTION: Brass screws.

6. Remove the perimeter screws (Figure 9.6, Step 3).

   CAUTION: At this point, the upper and lower interconnect boards are holding in the memory mother board. View the interconnect boards through the rear panel access cover (Figure 9.6, Step 4).

9.42 Installation

CAUTION: When reinstalling the memory mother board, the crucial point is in the alignment of the upper and lower interconnect boards.

2. When installing the memory mother board, align the pins on the lower connector first by pivoting the board from the top and, as the top of the board approaches the upper interconnect board, align the upper interconnect pins. View through the rear access cover, Figure 9.9, Step 4. Check pin alignment on the upper interconnect board with an inspection mirror through the rear access panel.

3. CAUTION: When installing the voltage transfer screws, do not force them. They are brass screws and therefore break easily. (See Figure 9.6, Step 3.)

4. Install perimeter screws (Figure 9.6, Step 3) and card guides (Figure 9.6, Step 2).

5. Install memory boards and clock generator. Check for correct installation on clock generator co-ax (Figure 9.6, Step 1).

6. Install plug-in.

9.5 Power Supply Conversion

9.51 110 V (See Figure 9.7, Step 1. See also Tektronix instruction manual, supplied for 603/604 Monitor, pages 1-3 and pullout number 4.)

1. Remove 8200 top cover.

2. Place the 110/220 power selector in the 110 VAC position.

3. With the Hi/Low line selector, match the AC line voltage. "N" position is for 100 VAC.

4. With the display Hi/Low, 110/220 selector, select the brown plug for 110 VAC operation. There are three positions for the plug. They read top-to-bottom, high-medium-low line voltage.

5. The correct fuse for the 604 display unit is a 1-A 3AG SLO BLO. The correct fuse for the 8200 is an AGC 2-A.

9.52 220 V (See Figure 9.7, Step 1.)

1. Remove 8200 top cover.

2. Place the 110/220 power selector in the 220 VAC position.

3. Match the line voltage for variance from 220. The "N" position is for 220 VAC operation.

4. Select the red plug for 220 V operation. The red 220 V plug is stored just below and to the front of the display Hi/Low 110/220 selector. Match the plug position for high-medium-low line operation from top to bottom.

5. Store the unused plug in the position just below and to the front of the display Hi/Low 110/220 selector that was left for plug storage.

6. The correct fuse, F840, for the 604 display unit is 1/2-A 3AG SLO BLO. The correct fuse for the 8200 is an AGC 2-A.

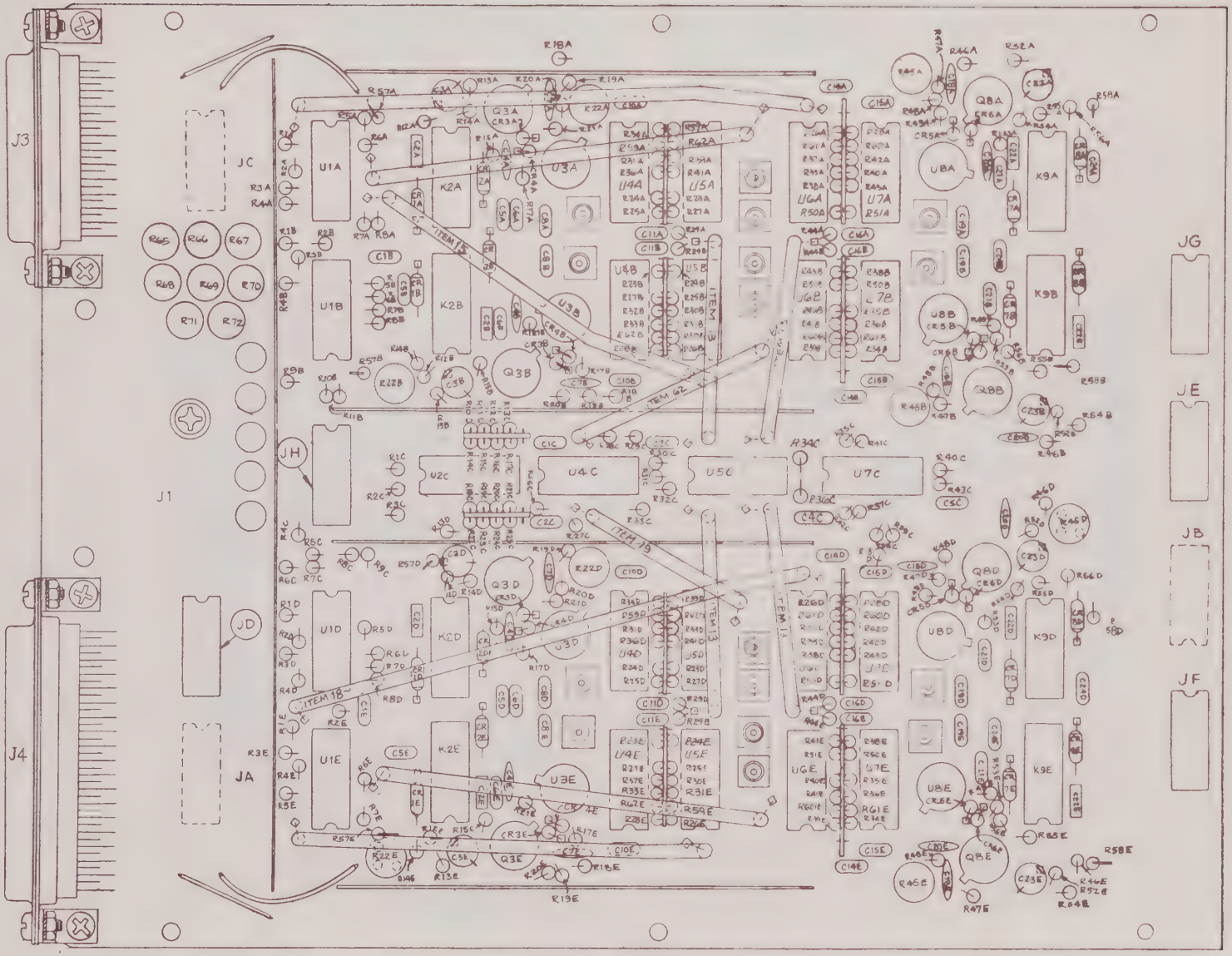


Figure 9.17 Assembly, Logic Board (8201-D)

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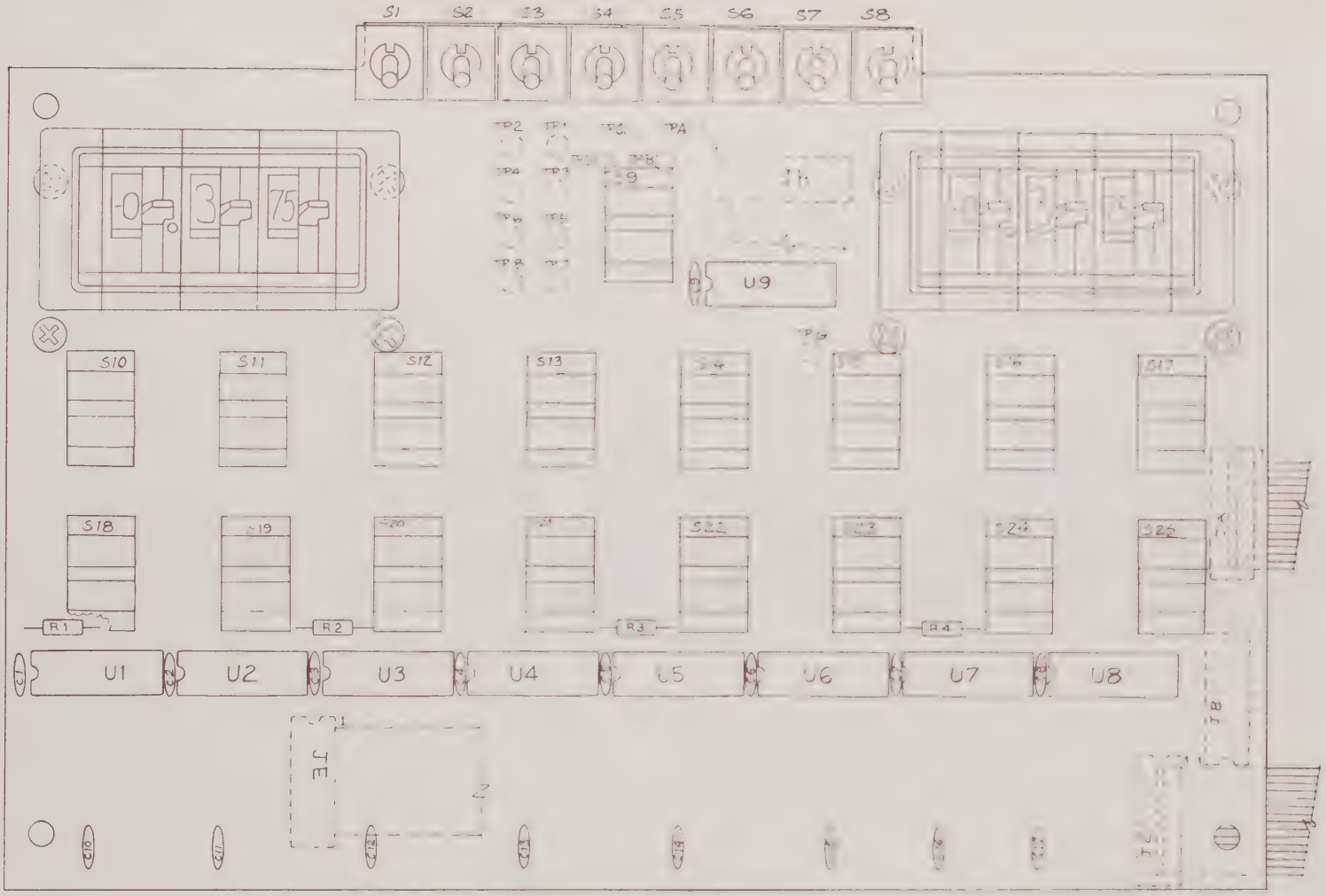


Figure 9.11 Assembly, Front Panel
(8201-D)

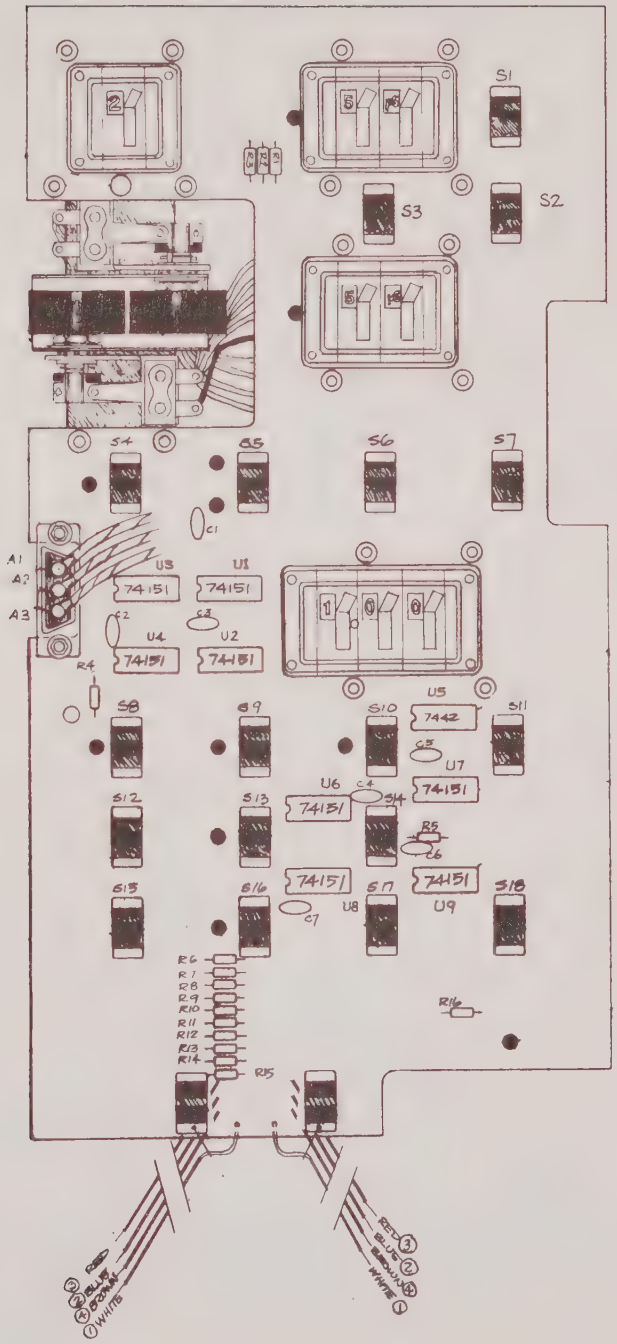


Figure 9.13 Assembly, Main Frame Front Panel

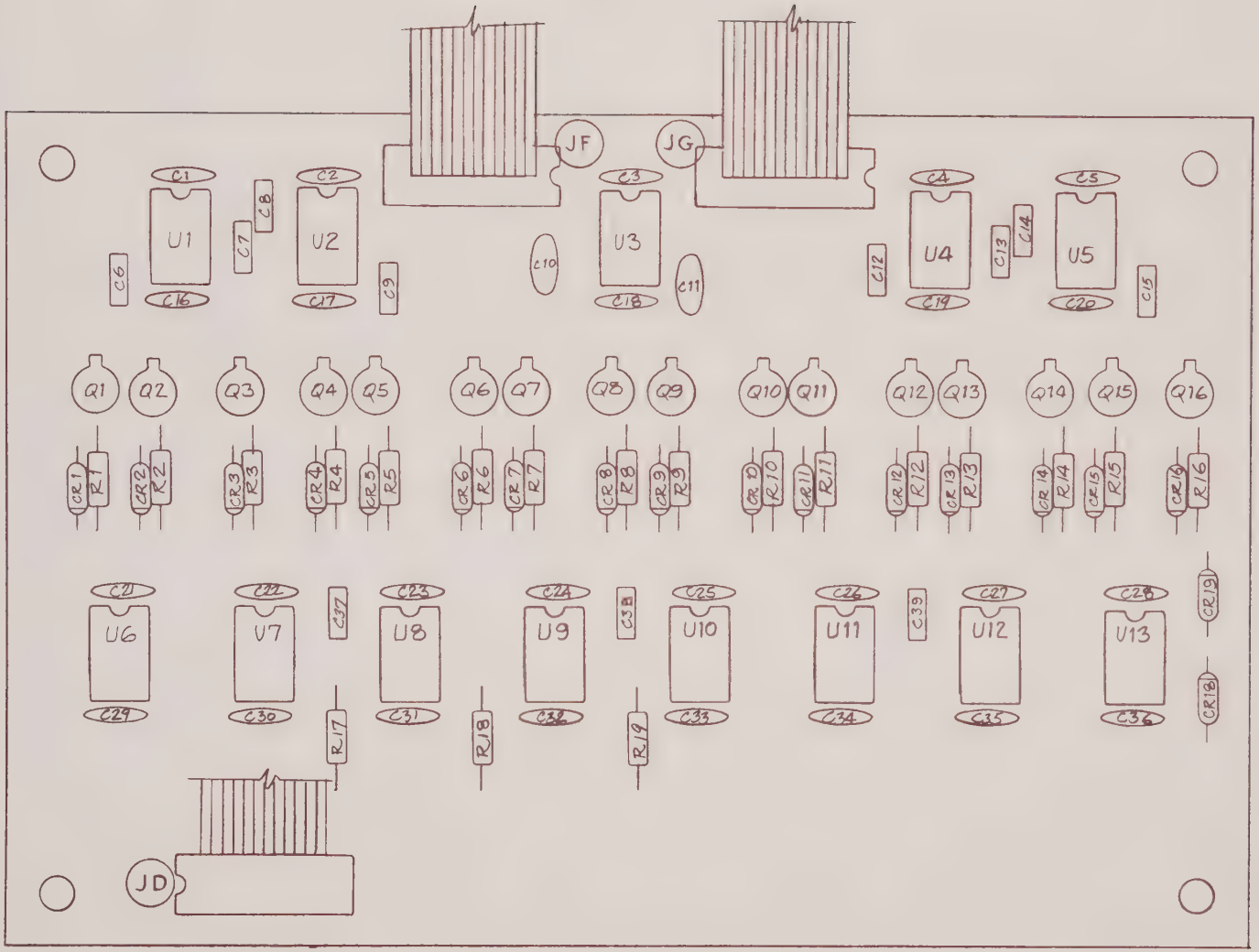


Figure 9.15 Assembly, Threshold Selector

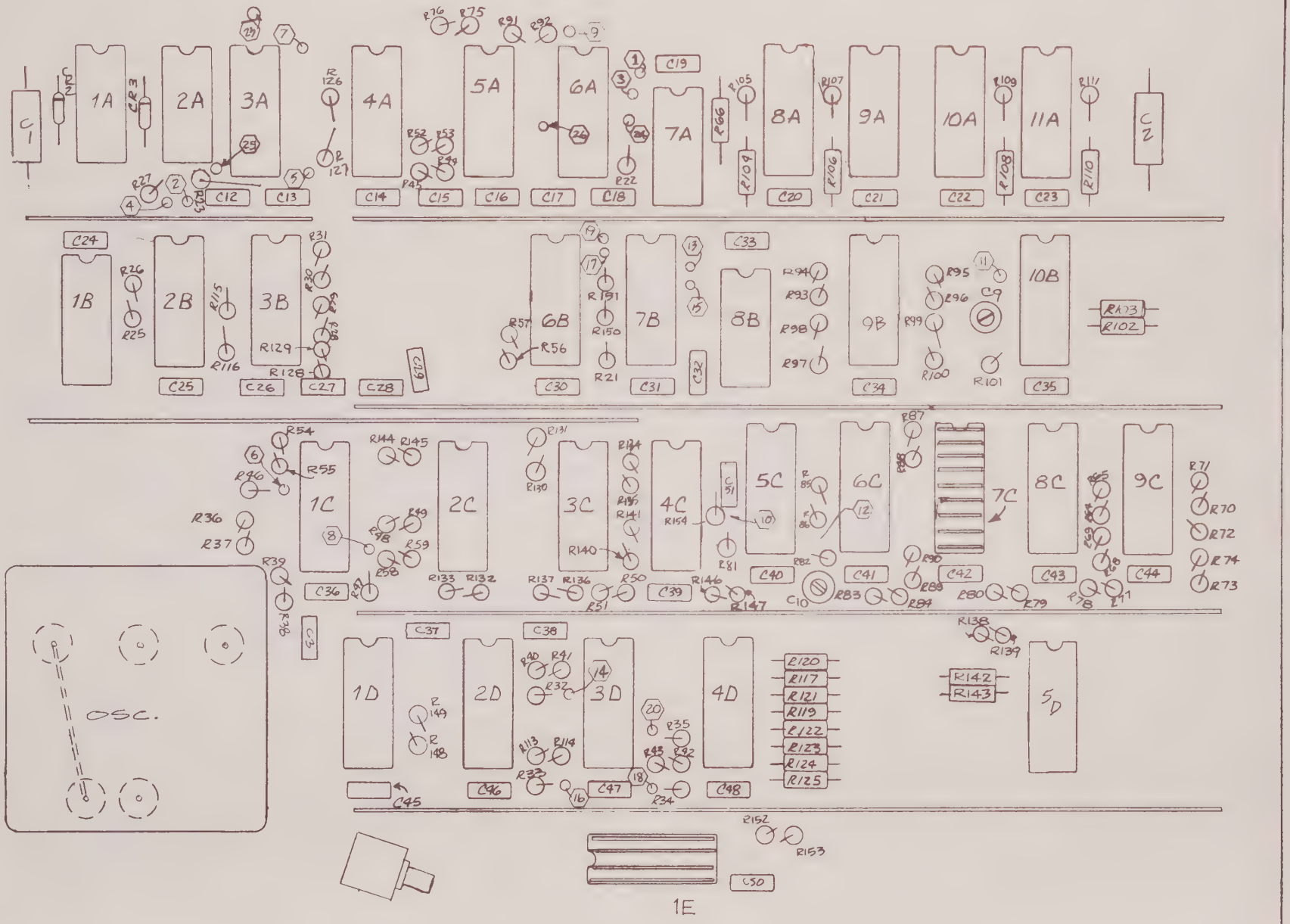


Figure 9.19 Assembly, Clock Generator

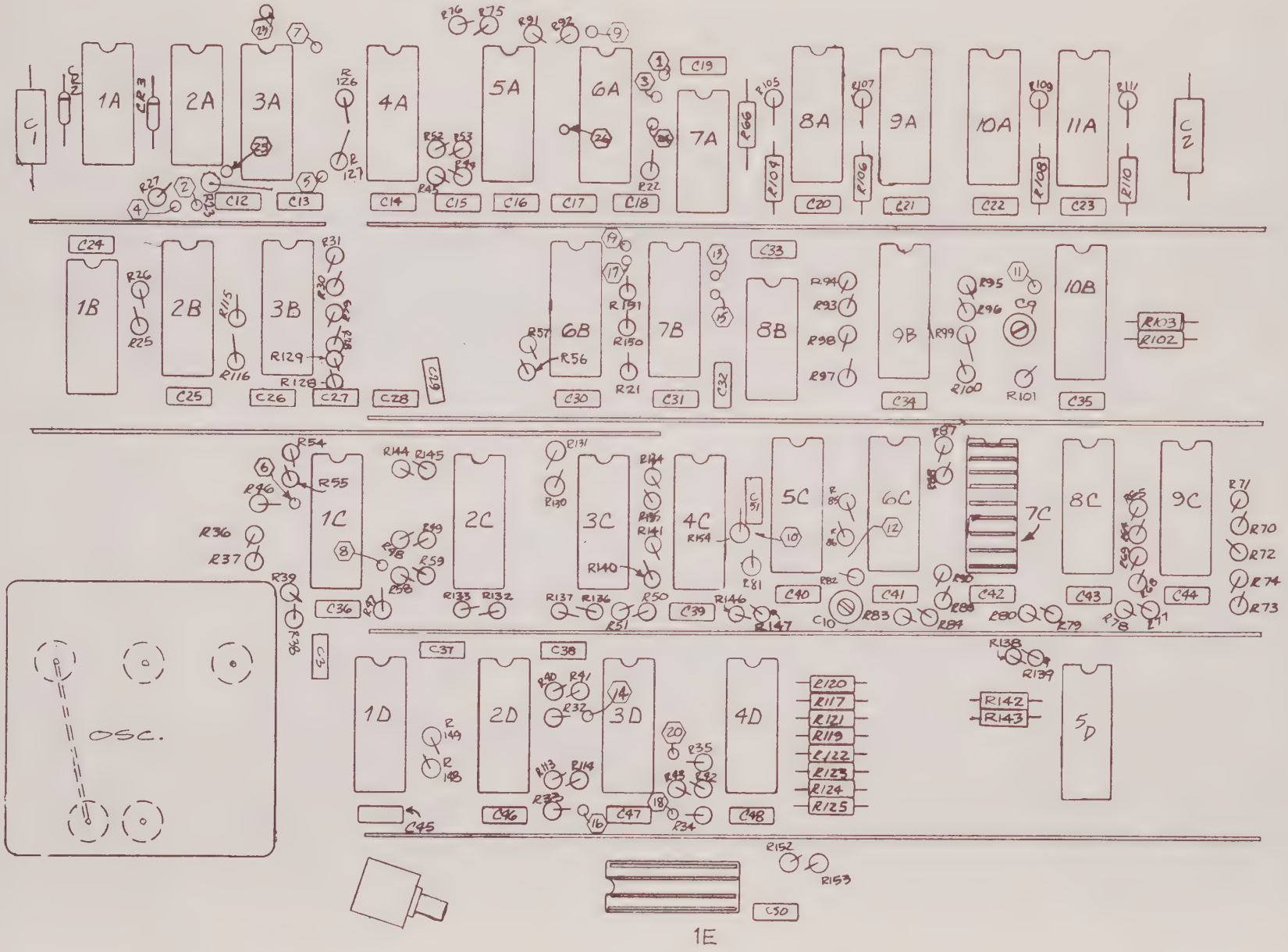


Figure 9.19 cont. Assembly, Clock Generator

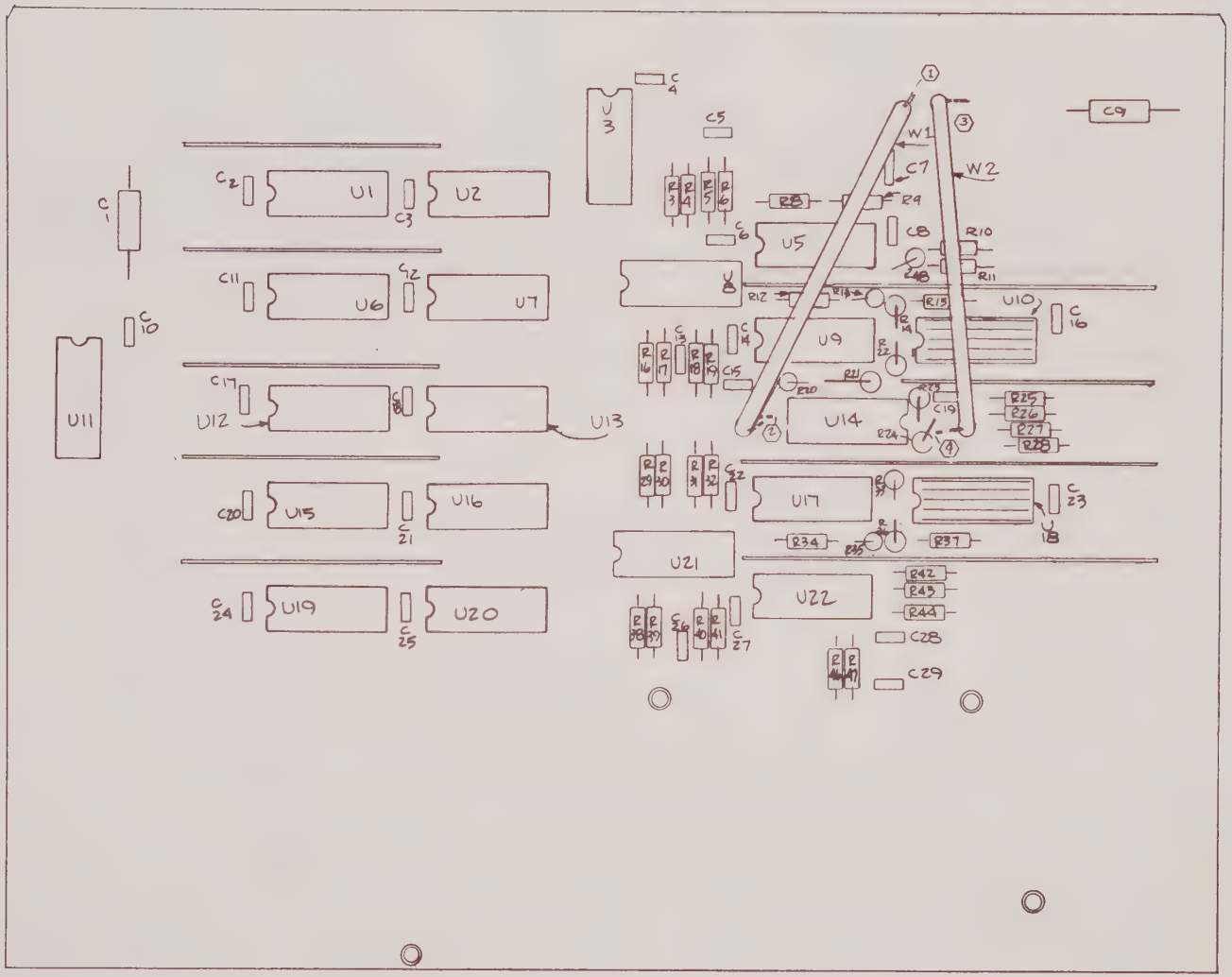


Figure 9.21 Assembly, Channel Memory

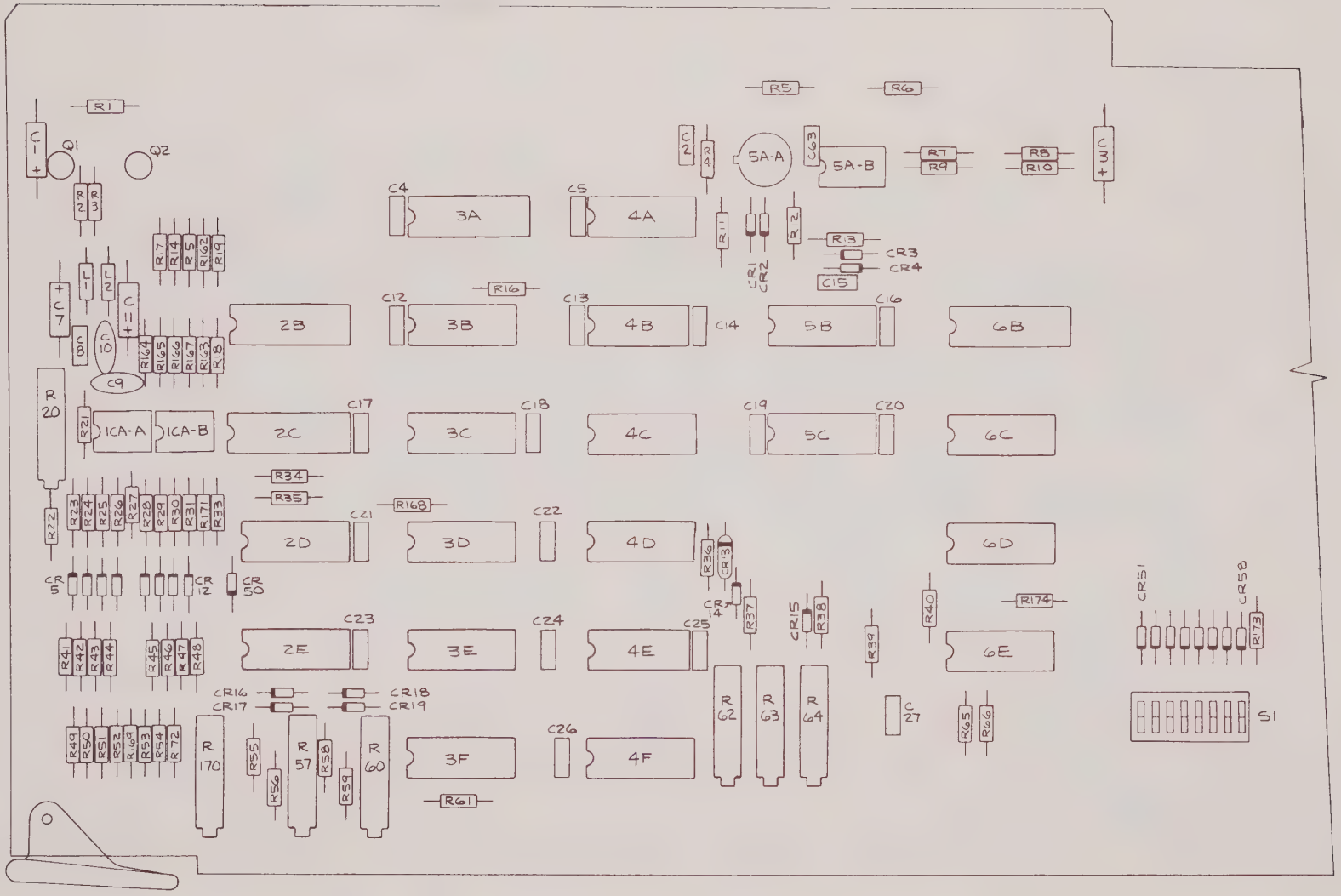


Figure 9.23 Assembly, Display Control Board

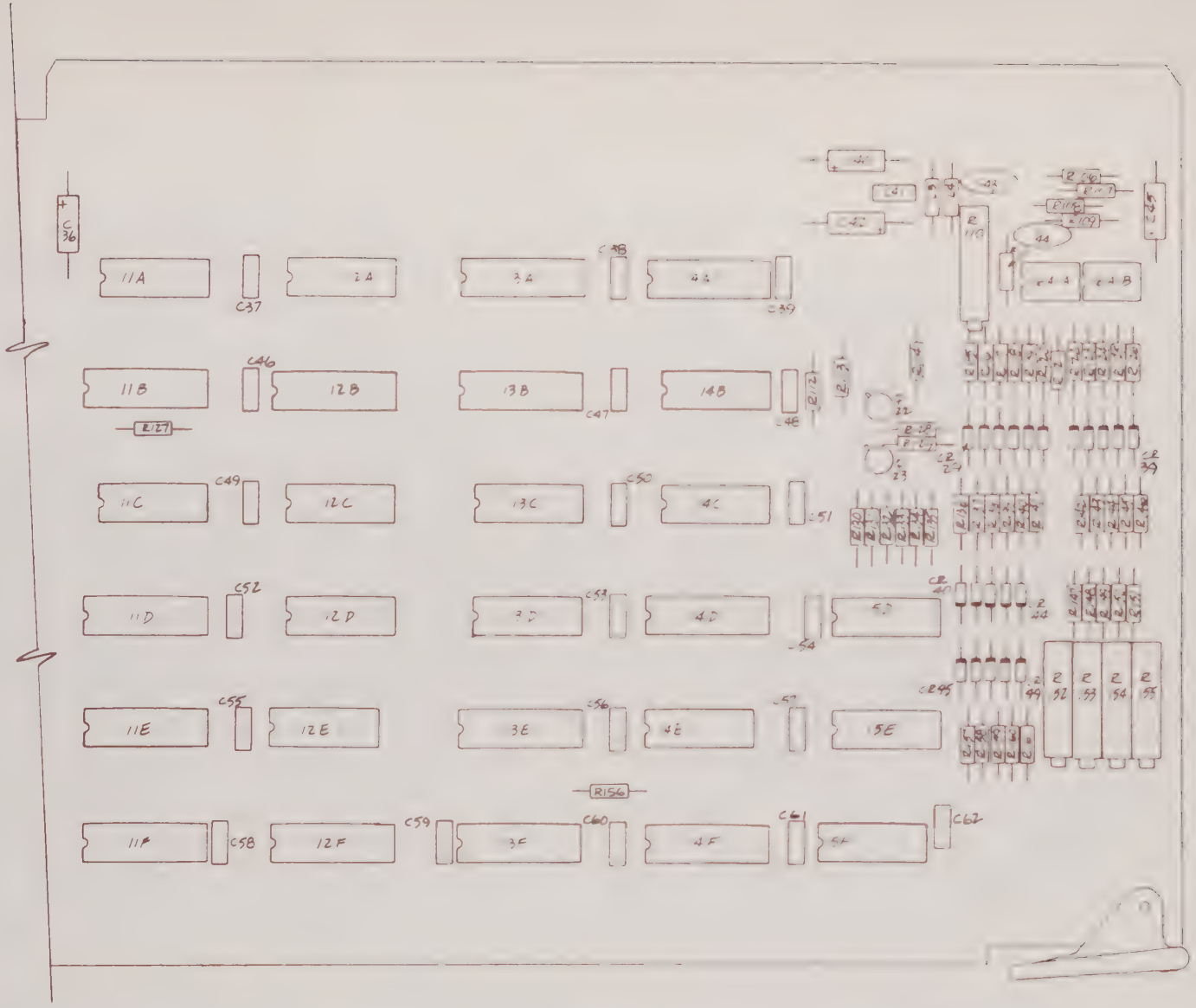


Figure 9.23 cont. Assembly, Display Control Board

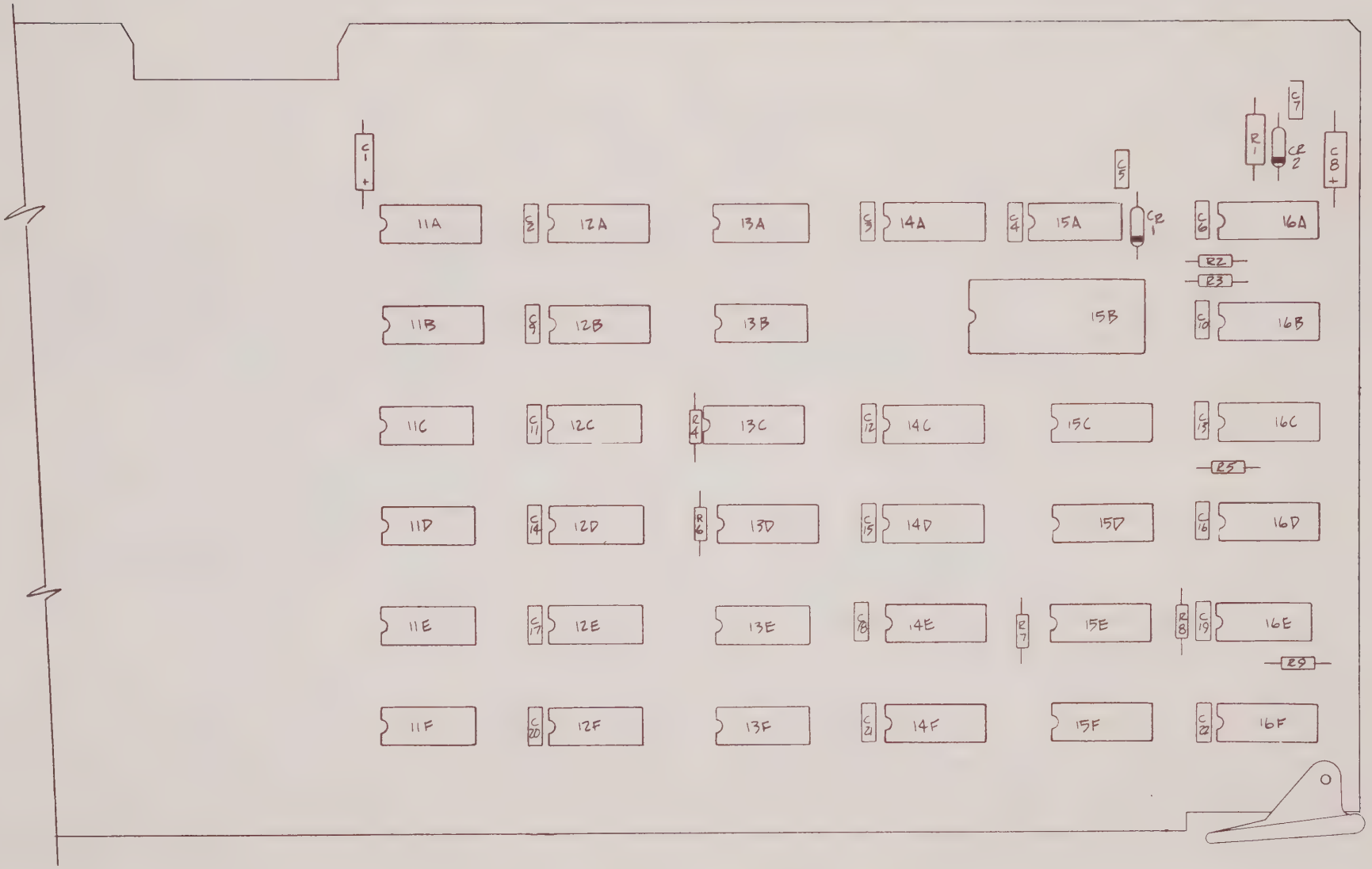


Figure 9.25 Assembly, Character Generator

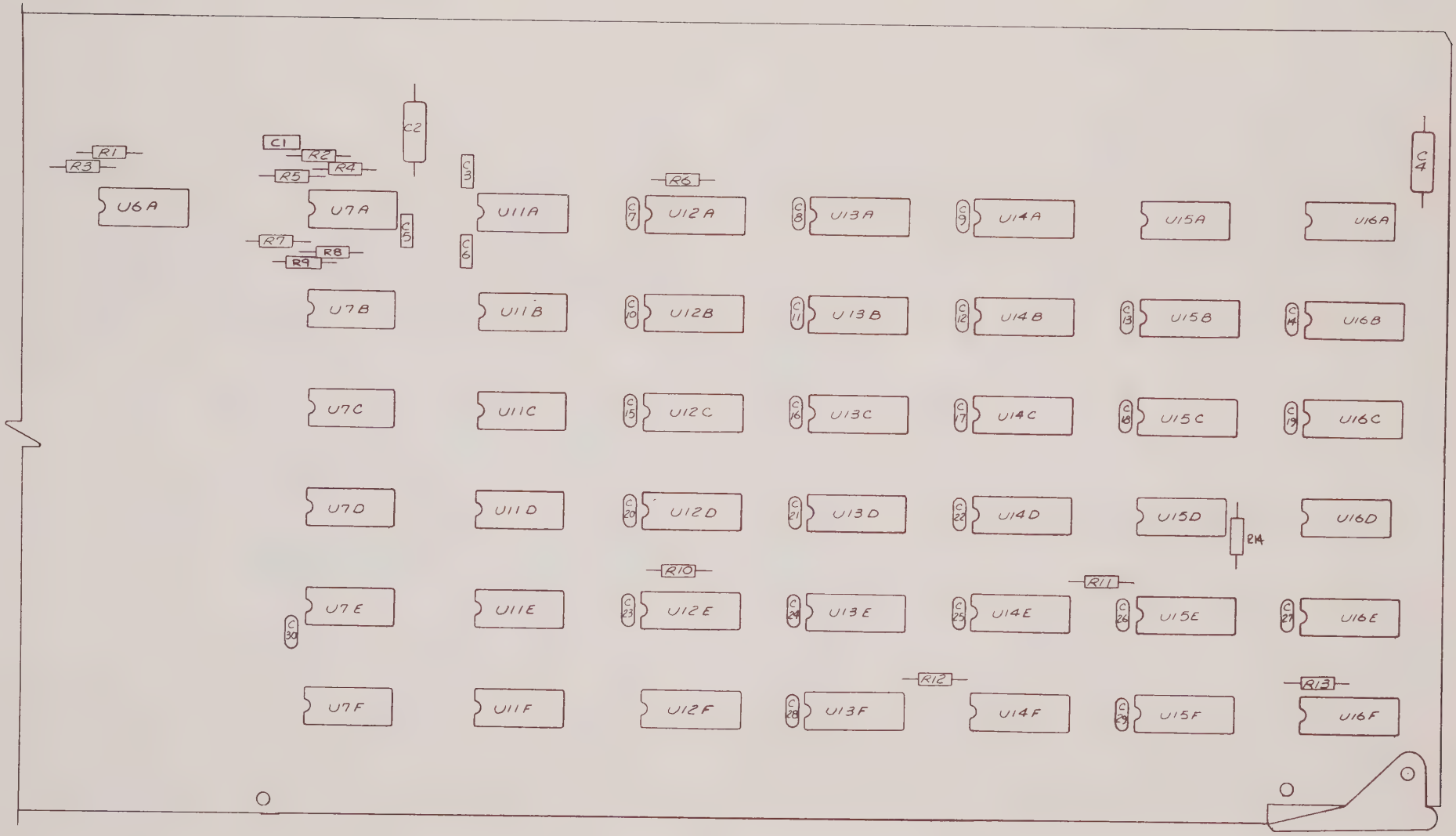


Figure 9.27 Assembly, Cursor Control Board

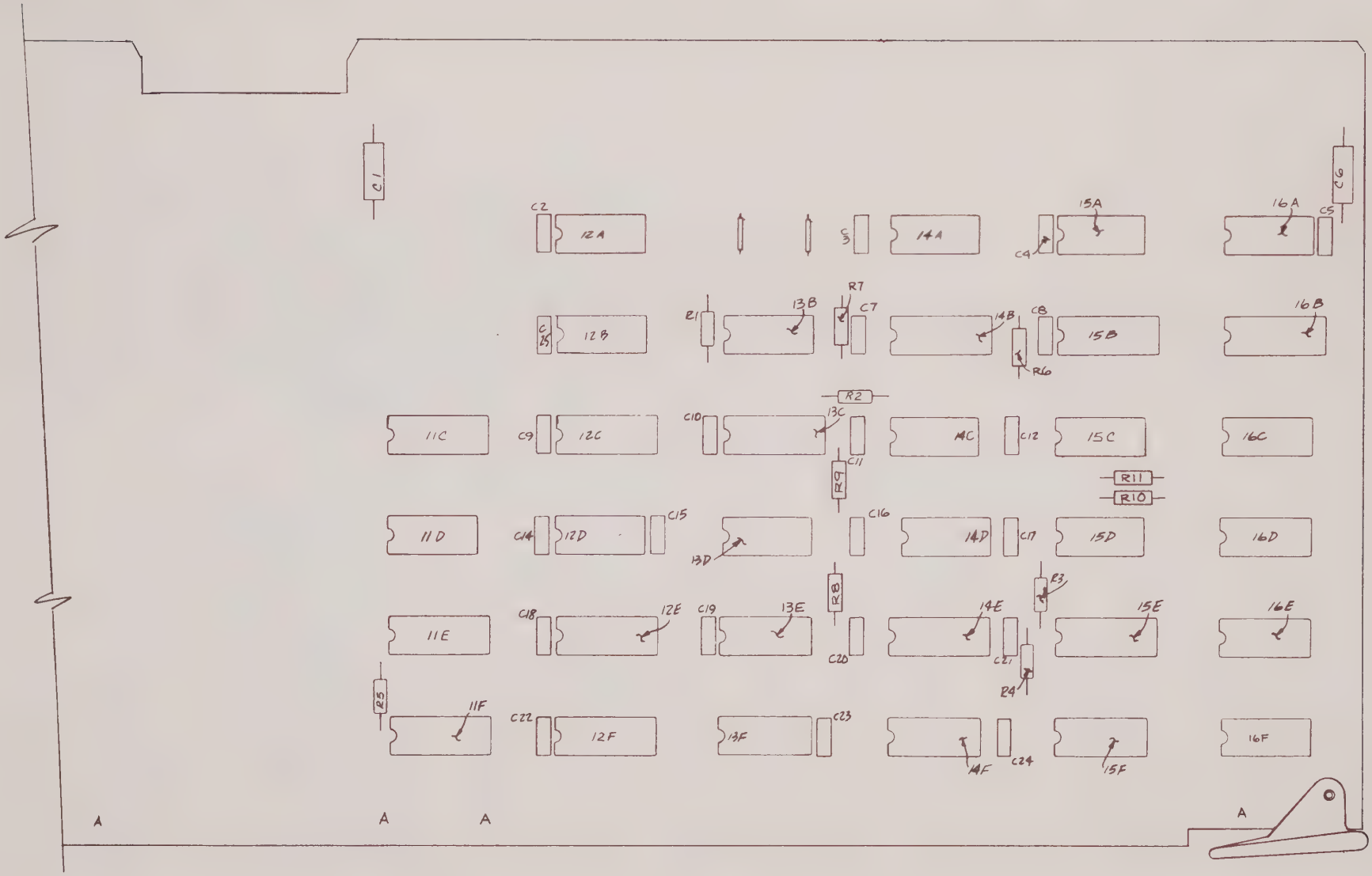


Figure 9.29 Assembly, Address Control Board

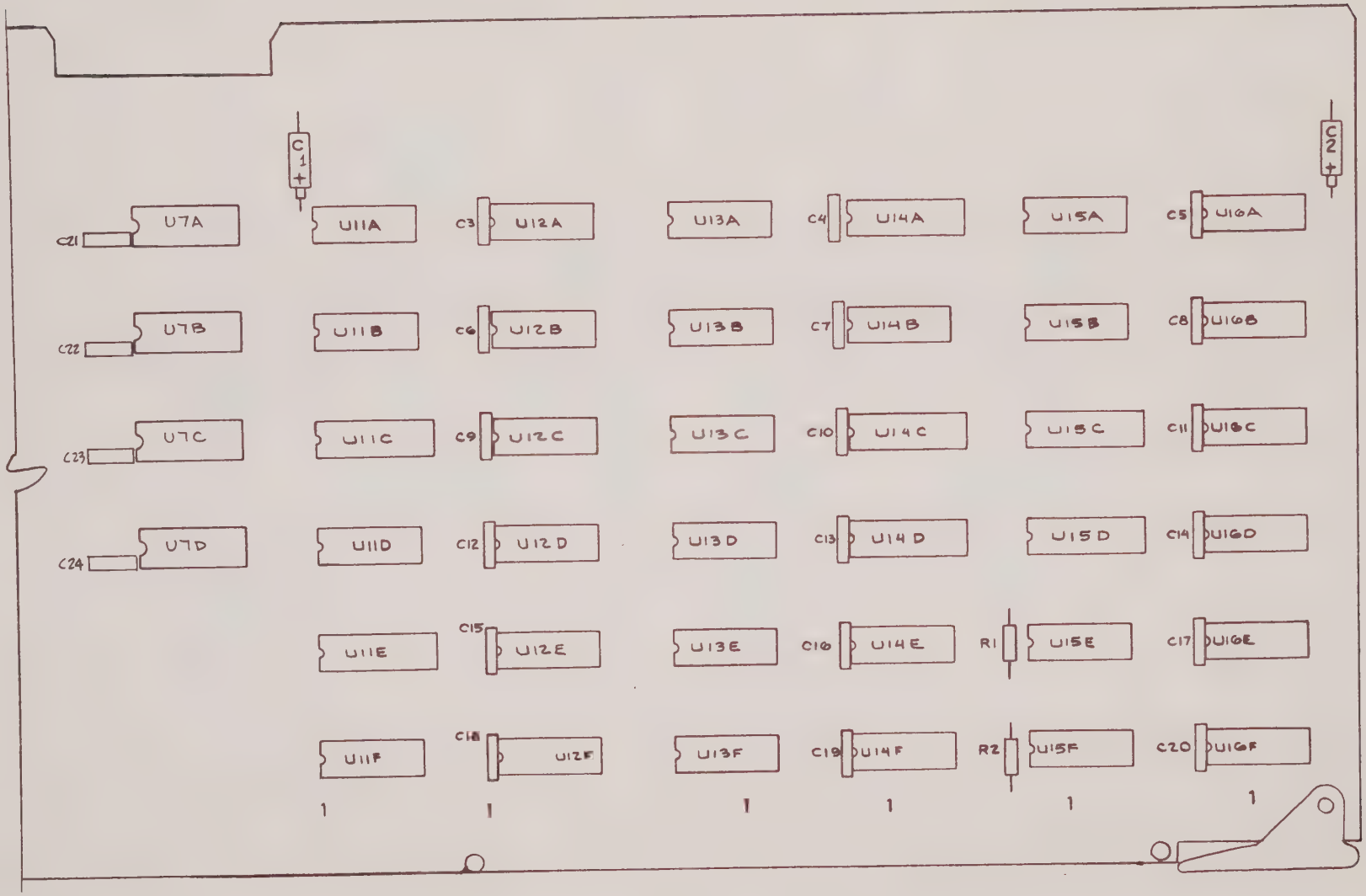


Figure 9.31 Assembly, Time Base

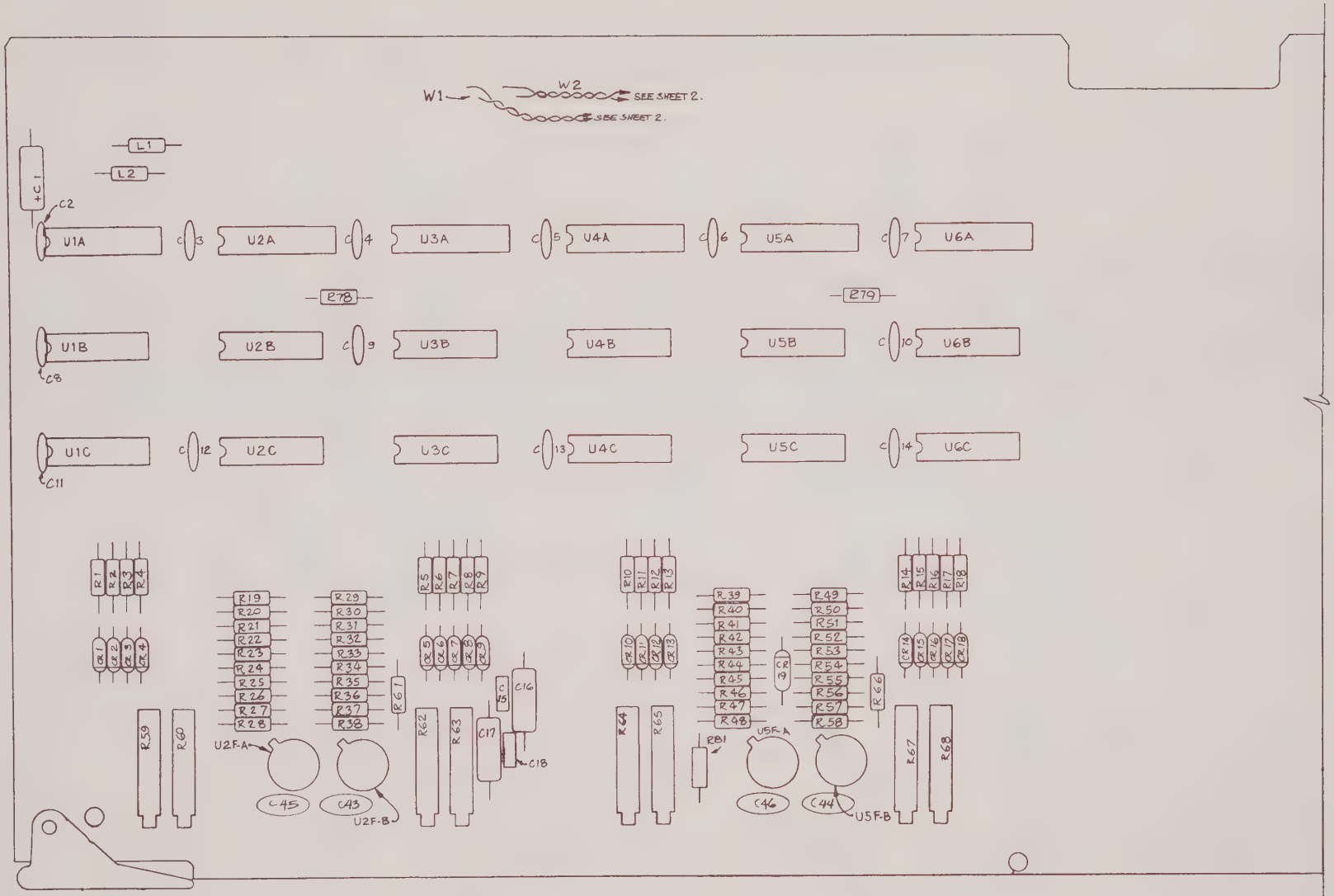


Figure 9.33 Assembly, Mode Control Board

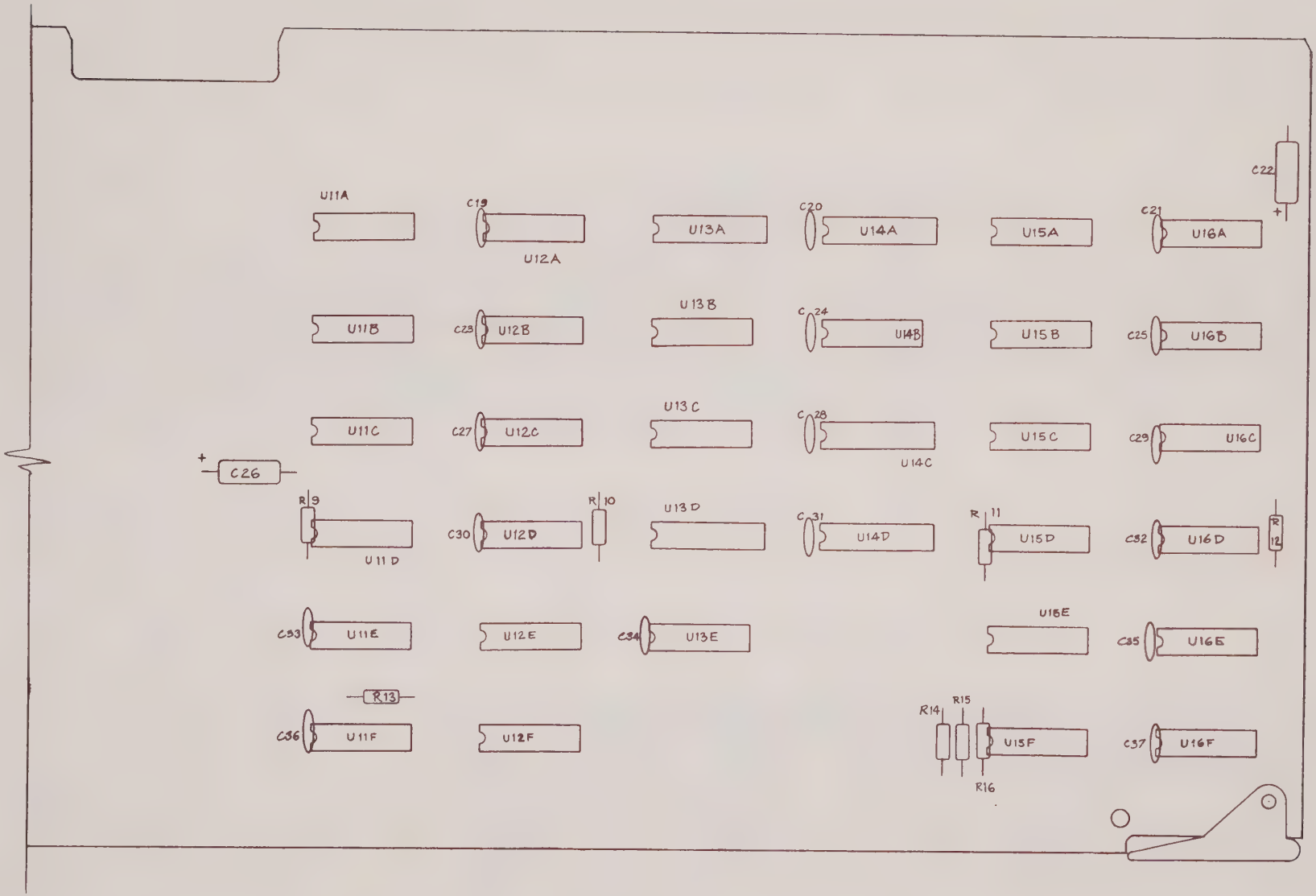


Figure 9.37 Assembly, Control Register

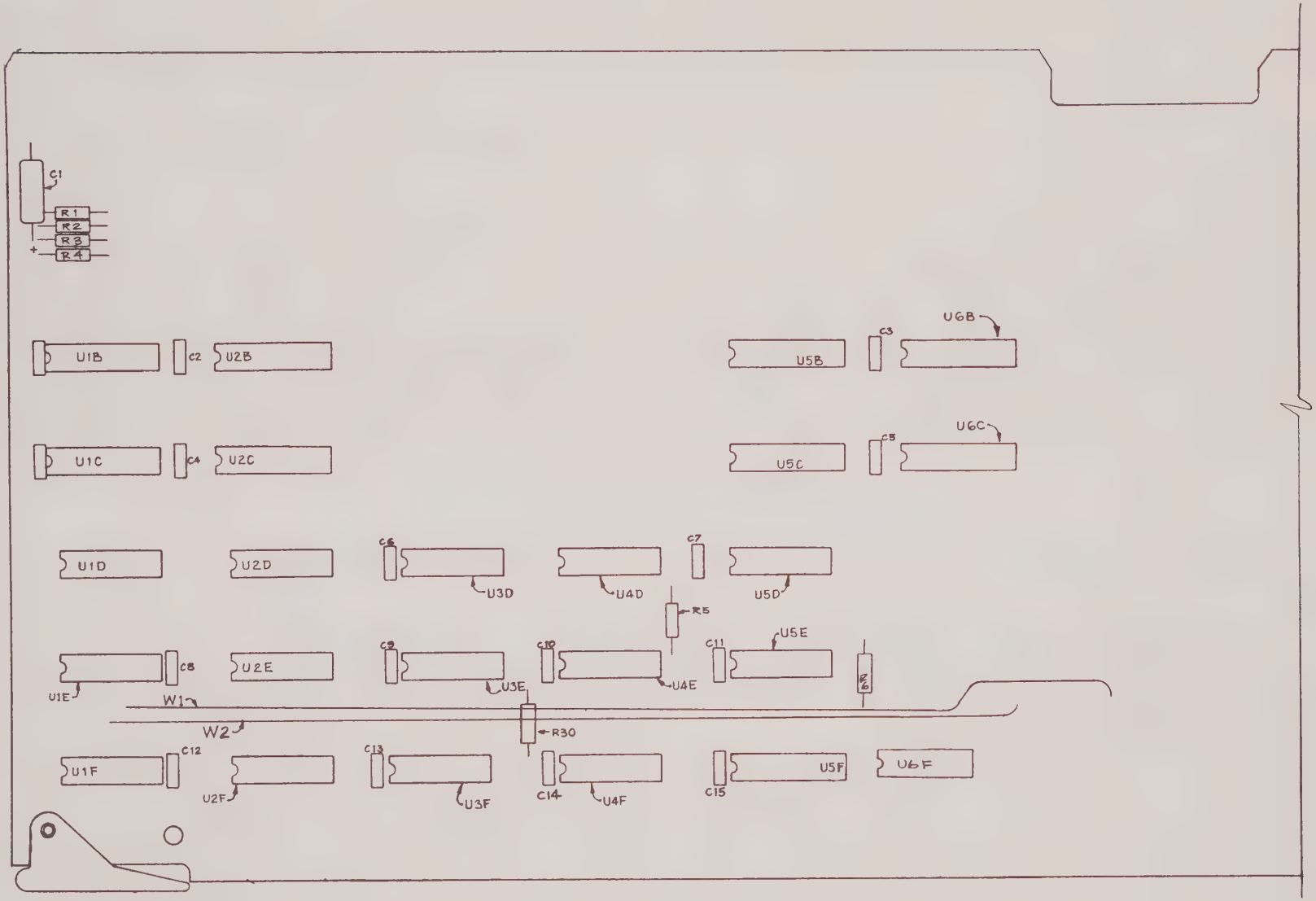


Figure 9.39 Assembly, Remote In/Remote Out

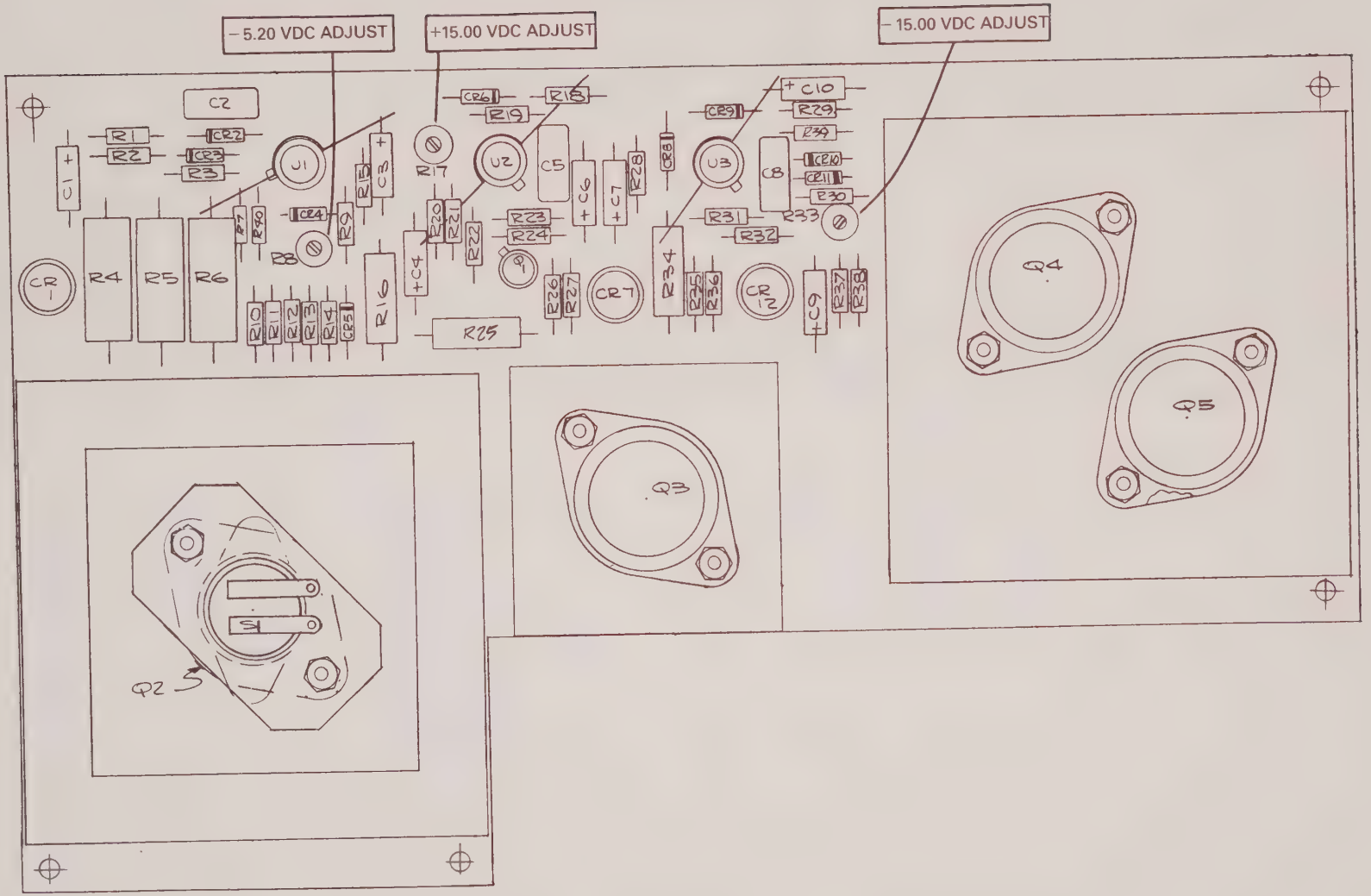
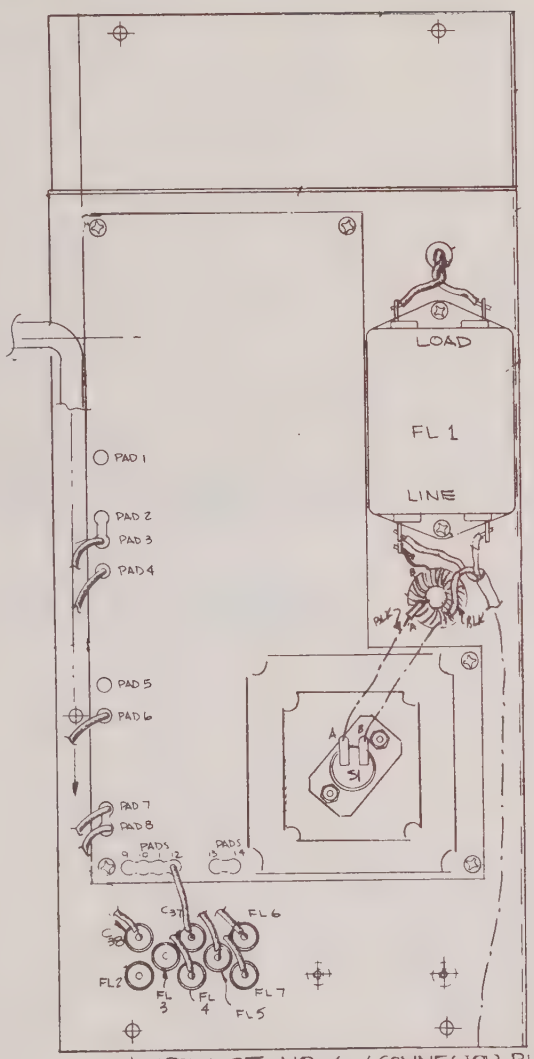


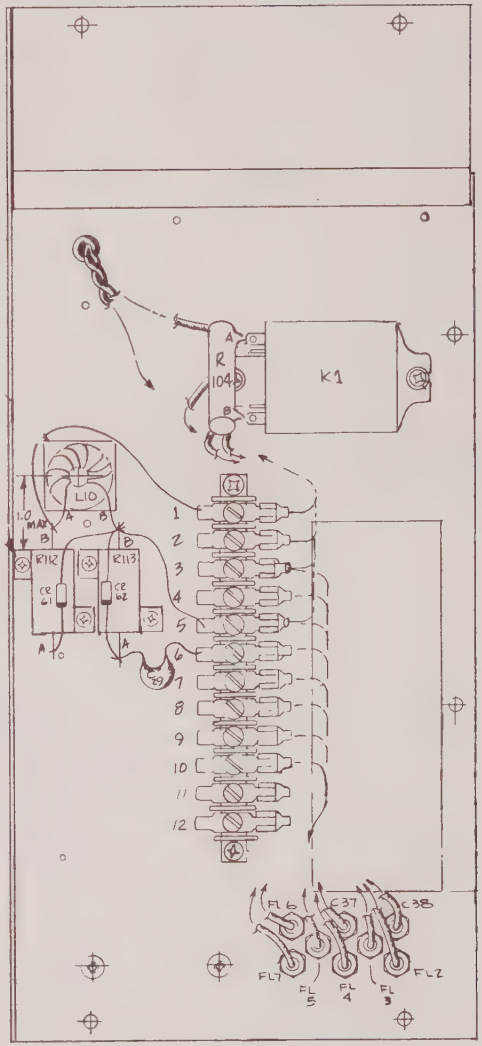
Figure 9.43 Assembly, Regulator Board



WIRE LIST

WIRE NO.	FROM	END TERM	TO	PAD OR TERM	COLOR
1	REG BD	3	C38	TOP SIDE	GRY
2		4	FL4		VIO
3		6	FL5		RED
4		7	FL6		GRN
5		8	FL7		GRN
6	REG BD	12	C37	TOP SIDE	BLU
7	LINE CABLE	WHT	FL1	A	—
8		BLK	S1	B	—
9	LINE CABLE	GRN	FL1	GND	—
10	FL1	D	TB-1	3	BLK
11	FL1	C	TB-1	4	WHT
12	RELAY (K1)	7	RELAY (K1)	9	BLK
13		9	R104	B	—
14		4	R104	A	—
15		4	RELAY (K1)	6	YEL
16		6	TB-1	1B	YEL
17		A	TB-1	9A	GRN
18	RELAY (K1)	B	TB-1	8A	BLU
19	TB-1	7A	FL2	BOT SIDE	ORN
20		7B	FL3		ORN
21		8B	C37		BLU
22		9B	FL6		GRN
23		9C	FL7		GRN
24		10	FL5		RED
25		11	FL4		VIO
26	TB-1	12	C38	BOT SIDE	GRY
27	S1	A	INDUCTOR	A	BLK
28	INDUCTOR(L9)	B	FL1	B	BLK
34	REGULATOR BD	1	CONNECTOR (J1)	H	VIO
35		2		20	GRY
36		5		6	RED
37		9		A	BLU
38		10		C	BLU
39		11		5	BLU
40		13		P	GRN
41	REGULATOR BD	14		14	GRN
42	FL2	TOP SIDE		K	ORN
43	FL3	TOP SIDE	CONNECTOR (J1)	10	ORN
44	RELAY (K1)	9	TB-1	2	BRN
58	TB-1	1A	R112	B	YEL
59	TB-1	5	R113	B	RED/WHT
60	R113	B	L10	B	—
61	R112	B	L10	A	—
62	R112	A	R113	B	CR61
63	R113	A	R113	B	CR62
64	R113	A	TB-1	6B	C29

BOTTOM VIEW



WIRE LIST NO. 6 (CONNECTOR BUSING)

WIRE NO.	CONNECTIONS	WIRE SIZE	FUNCTION
29	BUS CONN PINS B-11, J-M	#18 BUS	+5V
30	12-15, N-S		-5.2V
31	1-5, A-E, 18-22, V-Z		GND
32	7, H, 16, T		-15V
33	BUS CONN PINS 6, F, 17, U	#18 BUS	+15V

Figure 9.45 Assembly, Power Supply and Wire List

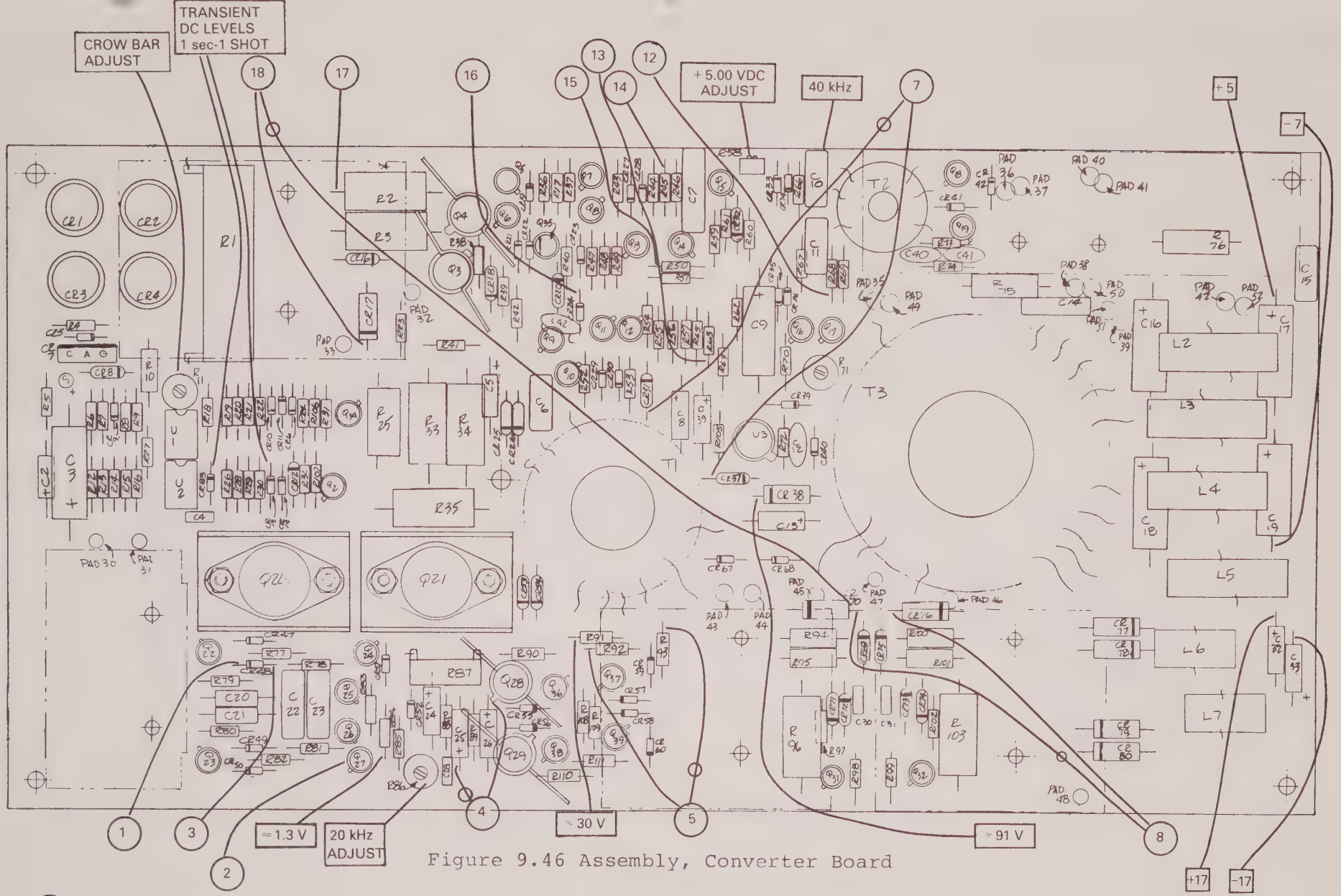


Figure 9.46 Assembly, Converter Board

6 BASES Q30, Q33

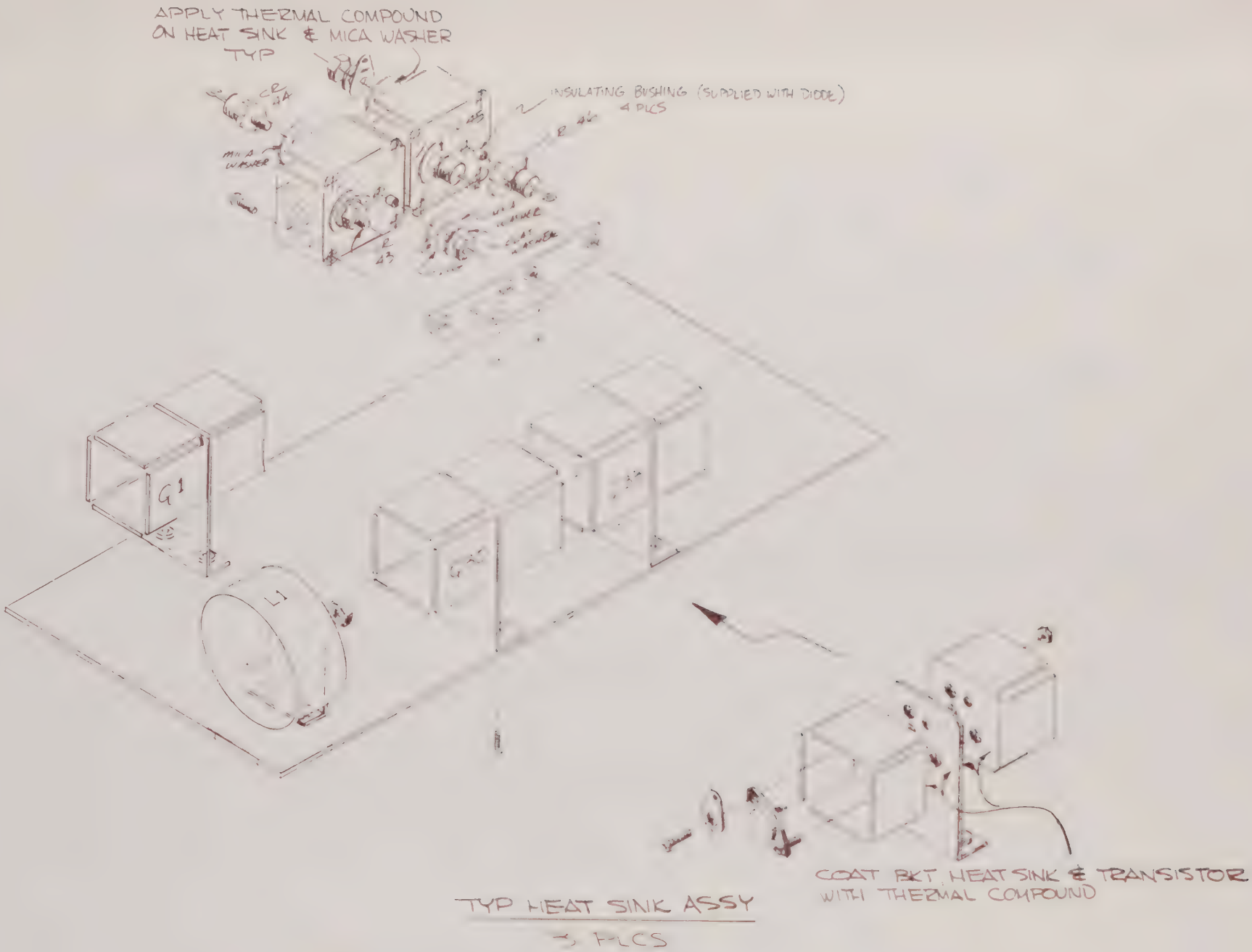


Figure 9.46 Cont. Assembly, Converter Board

NOTE: Operation of the 8200 power supply outside of the chassis Must Be *performed as follows:*

1. *An Isolation Transformer must be in between the AC mains and the Power Supply AC Input.*
2. *Suitable loads must be connected to the Power Supply outputs (As shown below).*

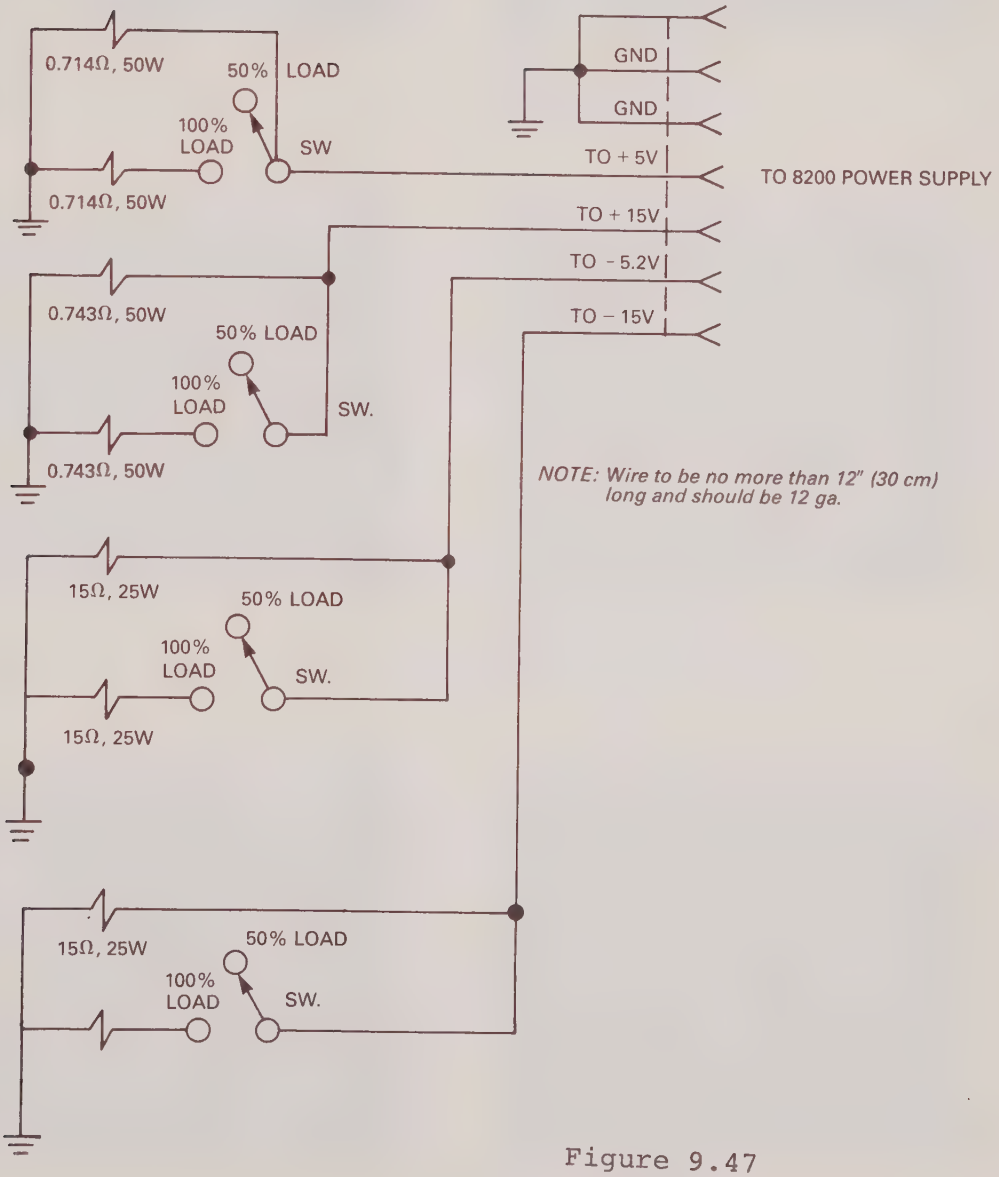
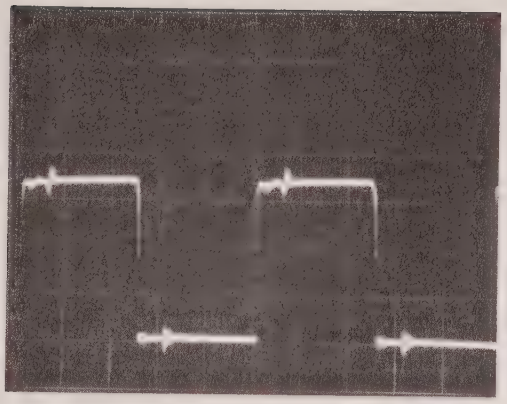
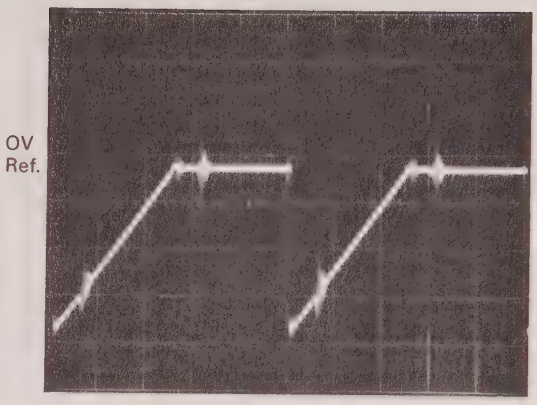


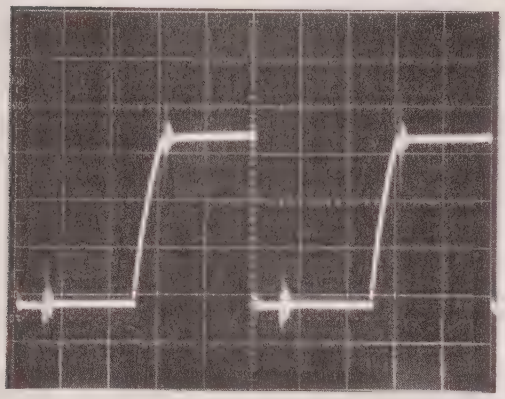
Figure 9.47
DC Load Schematic Diagram



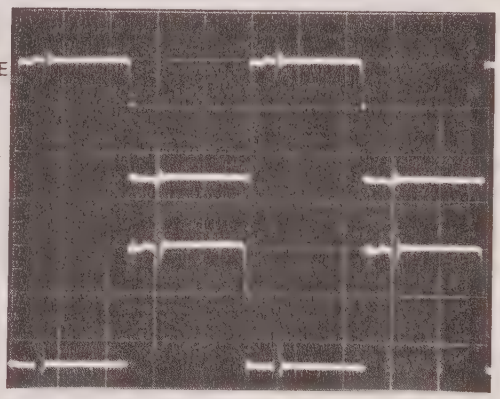
1. Scope: Vert. 2 V/div
Horz. 10 μsec/div
Trigger: Int, + Slope
NOTE: Scope GND to − side of C3



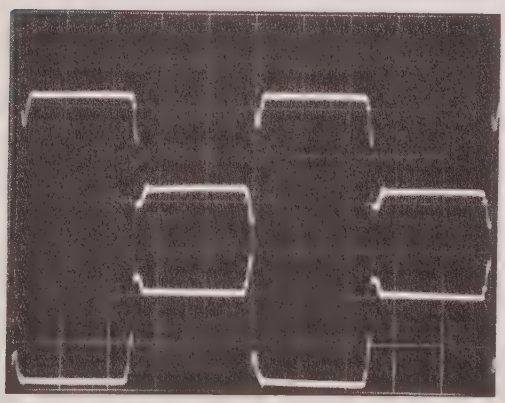
2. Scope: Vert. 1 V/div
Horz. 10 μsec/div
Trigger: Int, − Slope
NOTE: Scope GND to − side of C3



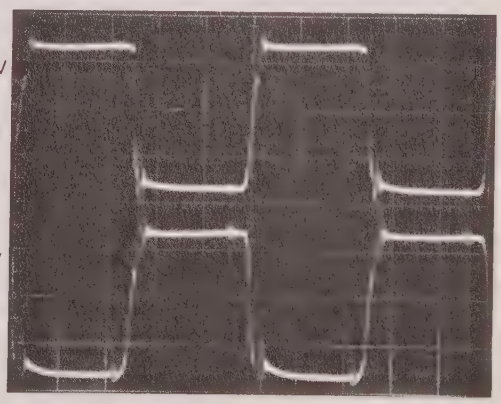
3. Scope: Vert. 1 V/div
Horz. 10 μsec/div
Trigger: Int, − Slope
NOTE: Scope GND to − side of C3



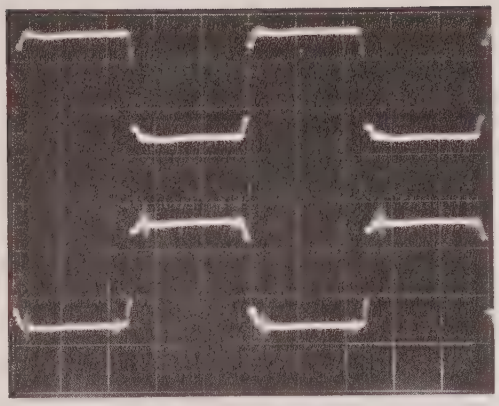
4. Scope: Vert. 2 V/div
Horz. 10 μsec/div
Trigger: Int, CH 1 + Slope
NOTE: Scope GND to − side of C3



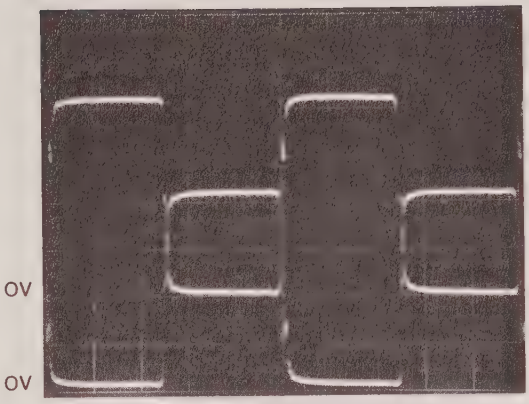
5. Scope: Vert. 50 V/div
Horz. 10 μsec/div
Trigger: Int, CH 1 + Slope
NOTE: Scope GND to − side of C3



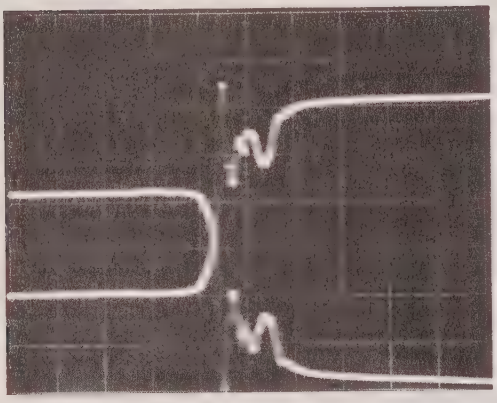
6. Scope: Vert. 2 V/div
Horz. 10 μsec/div
Trigger: Int, CH 1 + Slope
NOTE: Scope GND to − side of C3



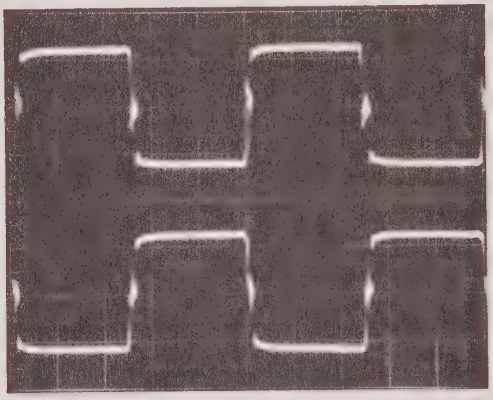
7. Scope: Vert. 10 V/div
Horz. 10 μsec/div
Trigger: Int, CH 1 + Slope
NOTE: Scope GND to + Side C9



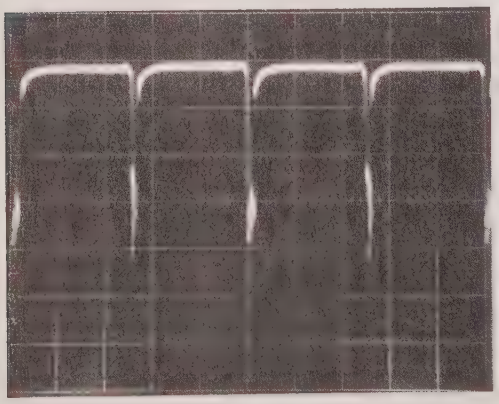
8. Scope: Vert. 50 V/div
Horz. 10 μsec/div
Trigger: Int, CH 1 + Slope
NOTE: Scope GND to − side of C3



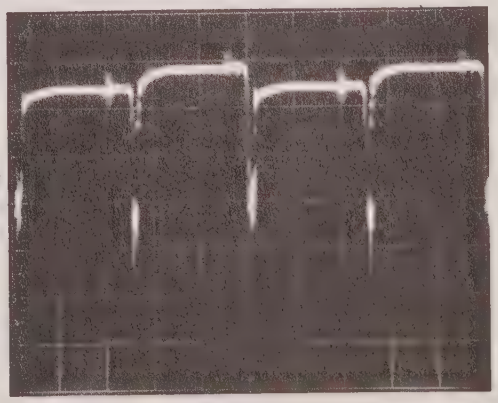
9. Scope: Vert. 50 V/div
Horz. Main 10 μsec.
Delayed 1 μsec
NOTE: Scope GND to − side of C3



10. Scope: Vert. 5 V/div
Horz. 10 μsec/div
Trigger: Int, CH 1 + Slope
NOTE: Scope GND to + 5 Return

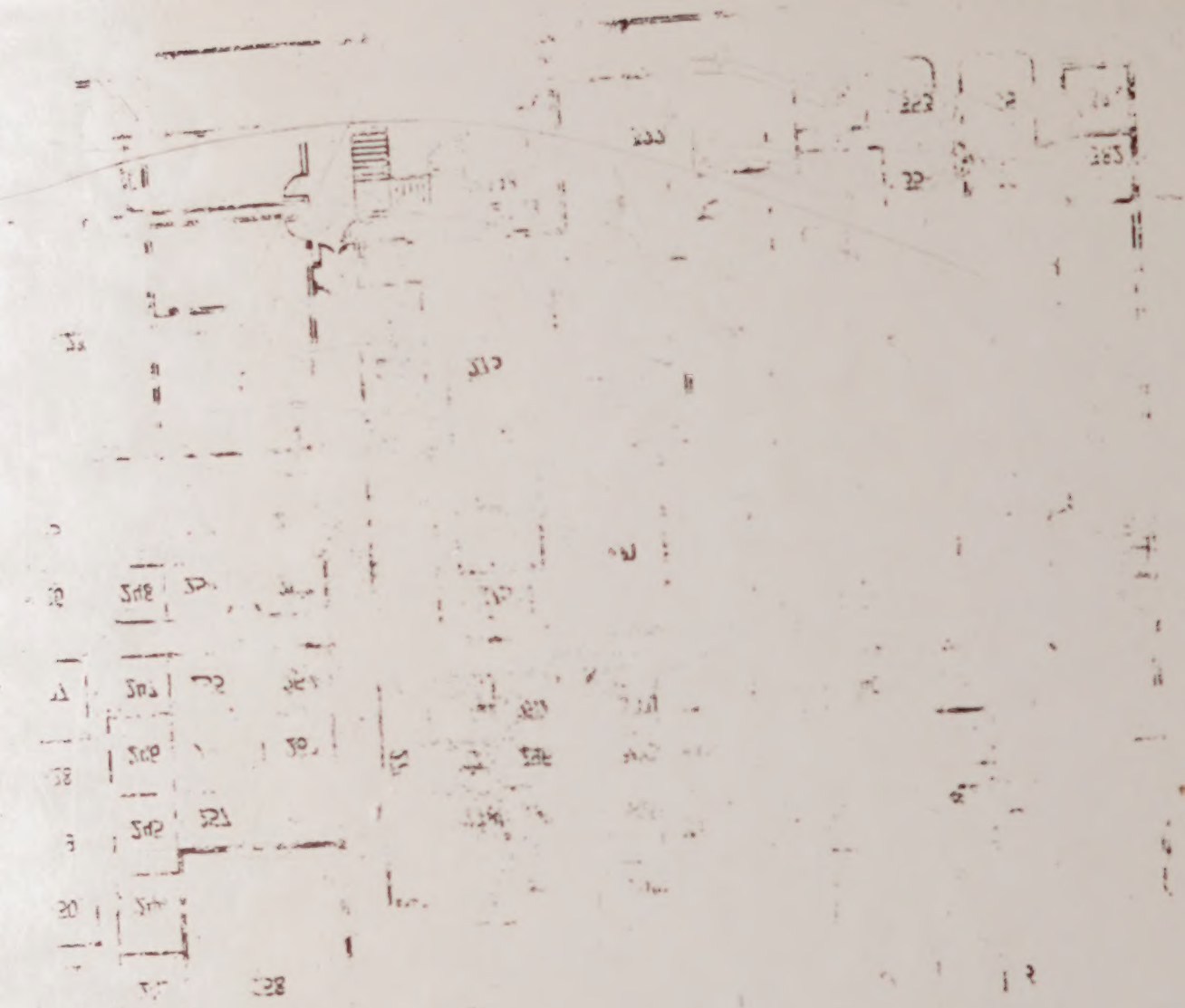


11. Scope: Vert. 2 V/div
Horz. 10 μsec/div
Trigger: Int, − Slope
NOTE: Scope GND to + 5 Return



12. Scope: Vert. 2 V/div
Horz. 10 μsec/div
Trigger: Int, − Slope
NOTE: Scope GND to + Side of C9

Warranty

All Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Biomation will pay all shipping charges relating to the repair of the unit. Units under warranty, buy beyond the thirty day period, should be sent to Biomation prepaid and Biomation will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF BIOMATION'S WARRANTY, BIOMATION SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL BIOMATION BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

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